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**UTILITY PATENT
APPLICATION TRANSMITTAL**(Only for new nonprovisional applications
under 37 CFR 1.53(b))

Attorney Docket No.

980268

Total Pages

First Named Inventor or Application Identifier

Kousuke SUZUKI and Katsuyuki KARAKAWA

Express Mail Label No.

Check Box, if applicable [] Duplicate

APPLICATION ELEMENTS FOR:

**SEMICONDUCTOR DEVICE HAVING A SELF-
ALIGNED CONTACT HOLE**ADDRESS TO: Assistant Commissioner for Patents
BOX PATENT APPLICATIONS
Washington, D.C. 20231

1. ☒ Fee Transmittal Form (Incorporated within this form)
(Submit an original and a duplicate for fee processing)
2. ☒ Specification Total Pages [45]
3. ☒ Drawing(s) (35 USC 113) Total Sheets [20]
4. ☒ Oath or Declaration Total Pages [2]
 - a. ☒ Newly executed (original)
 - b. ☐ Copy from prior application (37 CFR 1.63(d))
(for continuation/divisional with Box 17 completed).
 - i. ☐ Deletion of Inventor(s)
Signed statement attached deleting inventor(s) named in prior application,
see 37 CFR 1.63(d)(2) and 1.33(b).
5. ☐ Incorporation by reference (useable if box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under
Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby
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6. ☐ Microfiche Computer Program (Appendix)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)
 - a. ☐ Computer Readable Copy
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 - c. ☐ Statement Verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. ☒ Assignment Papers (cover sheet and document(s))
9. ☐ 37 CFR 3.73(b) Statement (when there is an assignee) ☒ Power of Attorney

**UTILITY PATENT
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PAGE 2 OF 3

10. ☐ English translation Document (if applicable)

11. ☒ Information Disclosure Statement ☒ Copies of IDS Citations (23 references)

12. ☒ Preliminary Amendment

13. ☒ Return Receipt Postcard (MPEP 503)

14. ☐ Small Entity Statement(s) ☐ Statement filed in prior application
Status still proper and desired.

15. ☒ Claim for Convention Priority ☐ Certified copy of Priority Document(s)

a. Priority of _____ application no. _____ filed on _____ is claimed under 35 USC 119.
The certified copies/copy have/has been filed in prior application Serial No. _____.
(For Continuing Applications, if applicable).

16. ☐ Other _____

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

☐ Continuation ☐ Division ☐ Continuation-in-part (CIP) of prior application no. ____/____

FEE TRANSMITTAL	Number Filed	Number Extra	Rate	Basic Fee
The filing fee is calculated below				\$ 790.00
Total Claims	41 - 20	21	x \$22.00	462.00
Independent Claims	6 - 3	3	x \$82.00	246.00
Multiple Dependent Claims			\$270 00	
Basic Filing Fee				1498.00
Reduction by 1/2 for small entity				
Fee for recording enclosed Assignment			\$40.00	40.00
TOTAL				\$1538.00

**UTILITY PATENT
APPLICATION TRANSMITTAL**

(Only for new nonprovisional applications
under 37 CFR 1.53(b))

Attorney Docket No

980268

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PAGE 3 OF 3

[XX] A check in the amount of \$1,538.00 is enclosed to cover the filing fee of \$1,498.00 and the assignment recordation fee of \$40.00.

[] Please charge our Deposit Account No. **01-2340** in the total amount of _____ to cover the filing fee and the _____ assignment recordation fee. A duplicate of this sheet is attached.

[XX] The Commissioner is hereby authorized to charge payment for any additional filing fees required under 37 CFR 1.16 or credit any overpayment to Deposit Account No. **01-2340**. A duplicate of this sheet is attached.

18. CORRESPONDENCE ADDRESS

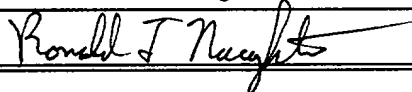
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Reg. No. 24,616

Signature



Date: March 20, 1998

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Kousuke SUZUKI et al.

Serial No.: Not Yet Assigned

Filed: March 20, 1998

For: SEMICONDUCTOR DEVICE HAVING A SELF-ALIGNED CONTACT HOLE

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

March 20, 1998

Sir:

Prior to the calculation of the filing fees of the above application, please amend the application as follows:

IN THE CLAIMS:

Claim 38, at line 1, delete "38" and substitute therefor --37--.

Claim 39, at line 1, delete "39" and substitute therefor --38--.

Claim 40, at line 1, delete "40" and substitute therefor --39--; and in line 2, delete "39" and substitute therefor --38--.

Claim 41, at line 1, delete "41" and substitute therefor --40--; and in line 2, delete "39" and substitute therefor --38--.

Claim 42, at line 1, delete "42" and substitute therefor --41--; and in line 2, delete "41" and substitute therefor --40--.

SECRET

In the event there are any additional fees required, please charge our Deposit Account
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ARMSTRONG, WESTERMAN, HATTORI,
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RFN/yap

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SPECIFICATION

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT WE, Kousuke Suzuki, a citizen of Japan residing at Kawasaki-shi, Kanagawa, Japan and Katsuyuki Karakawa, a citizen of Japan residing at Kasugai-shi, Aichi, Japan have invented certain new and useful improvements in

SEMICONDUCTR DEVICE HAVING A SELF-ALIGNED CONTACT HOLE

of which the following is a specification : -

1 TITLE OF THE INVENTION

SEMICONDUCTOR DEVICE HAVING A SELF-ALIGNED
CONTACT HOLE

5 BACKGROUND OF THE INVENTION

The present generally relates to
semiconductor devices and more particularly to a
miniaturized high-speed semiconductor device and a
fabrication process thereof.

10 With the development in the art of device
miniaturization, the operational speed of field-effect
semiconductor devices such as a MOS transistor is
increasing every year. On the other hand, such an
extremely miniaturized semiconductor device tends to
15 suffer from the problem of so-called short-channel
effect, which appears conspicuously in such a
miniaturized device having a short gate length, due to
the deviation from the classical gradual channel
approximation model. When a short-channel effect
20 appears, there arise problems such as deviation of
threshold voltage. In the worst case, the drain
current becomes no longer controllable by the gate
voltage.

Thus, it has been practiced in conventional
25 miniaturized field effect semiconductor devices to
reduce the thickness of diffusion regions as small as
possible in correspondence to the reduced gate length
of the device.

As such an extremely shallow diffusion
30 region tends to cause a problem of increased
resistance, it is proposed to provide a layer of low-
resistance silicide such as CoSi_2 on the surface of
the diffusion region by conducting a self-aligned
process. See for example Japanese Laid-Open Patent
35 Publication 7-115198.

Meanwhile, there is proposed a process of
forming an extremely miniaturized semiconductor device

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1 that includes a self-aligned contact structure. See
for example Japanese Laid-Open Patent Publication 8-
274278.

FIGS.1A - 1H show the foregoing conventional
5 process of forming a self-aligned contact structure.

Referring to FIG.1A, a gate oxide film 2 and
a field oxide film 2A are formed on a p-type Si
substrate 1, and a polysilicon layer 3 is deposited on
the structure of FIG.1A in the step of FIG.1B. The
10 polysilicon layer 3 thus deposited is then doped to
the n^+ -type by an ion-implantation of P^+ ions and
patterned in the step of FIG.1C to form a gate
electrode 3A. In the step of FIG.1C, an ion
implantation process of As^+ is further conducted while
15 using the gate electrode 3A as a mask, to form shallow
diffusion regions 1A and 1B of the n^+ -type at both
lateral sides of the gate electrode 3A by a self-
alignment process.

Next, in the step of FIG.1D, an SiO_2 film is
20 deposited on the structure of FIG.1C uniformly by a
CVD process, followed by an anisotropic etching
process acting substantially perpendicularly to the
surface of the substrate 1 to form side wall oxide
films 3a and 3b on both side walls of the gate
25 electrode 3A. Further, additional diffusion regions
1C and 1D are formed so as to partially overlap the
diffusion region 1A or 1B by conducting an ion-
implantation process of As^+ while using the gate
electrode 3A and the side-wall oxide films 3a and 3b
30 as a mask, to form a so-called LDD (lightly doped
drain) structure.

Next, in the step of FIG.1E, an SiN film 4
is deposited uniformly on the structure of FIG.1D by a
CVD process or a sputtering process, followed by the
35 step of FIG.1F in which an interlayer insulation film
5 of SiO_2 , PSG or BPSG is deposited on the foregoing
SiN film 4. The interlayer insulation film 5 is

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1 further formed with a contact hole 5A in
correspondence to the diffusion region 1C by an
anisotropic dry etching process. Similarly, a contact
hole 5B is formed in the insulation film 5 in
5 correspondence to the diffusion region 1D. The
contact hole 5A or 5B may be formed with a size
sufficiently larger than the size of the corresponding
diffusion region 1C or 1D and can be formed easily by
a photolithography without experiencing a difficulty
10 of resolution limit, which generally arises when
forming a deep contact hole.

The dry etching process for forming the
contact holes 5A and 5B stops spontaneously upon the
exposure of the underlying SiN layer 4 as indicated in
15 FIG.1F. Thus, a step of FIG.1G is conducted for
removing the exposed SiN film 4 by an etching process.
Further, a step of FIG.1H is conducted for removing a
part of the gate oxide film 2 that is now exposed at
the bottom of the contact holes 5A and 5B, by
20 conducting a selective etching process with respect to
the Si substrate 1. As a result of the step of
FIG.1H, minute openings 1c and 1d respectively
exposing the diffusion regions 1C and 1D are formed.

It should be noted that the opening 1c is
25 defined by the field oxide film 2A and the side wall
oxide film 3a. Similarly, the opening 1d is defined
by the other field oxide film 2A and the side wall
oxide film 3b. In other words, the openings 1c and 1d
are formed in a self-aligned manner, without using a
30 mask process. This means that the openings 1c and 1d
can be formed reliably and with reproducibility
without restrained from the problem of resolution
limit of exposure even when the semiconductor device
is extremely miniaturized. Further, as explained
35 already, it is not necessary to miniaturize the
contact holes 5A and 5B. Thus, the photolithography
for forming the contact holes 5A and 5B can be

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1 conducted easily.

Thus, the foregoing self-aligned process of
FIGS.1A - 1H is advantageous for forming extremely
miniaturized semiconductor devices. As already noted,
5 it is desired in such extremely miniaturized high-
speed semiconductor devices to form a low-resistance
silicide layer on the surface of the diffusion regions
1C and 1D so as to compensate for the unwanted
increase of the resistance, which tends to occur in
10 such extremely shallow diffusion regions.

One possibility of forming such a silicide
layer may include the steps of: removing the gate
oxide film 2 for the part covering the diffusion
regions 1C and 1D; depositing a metal layer of Co or
15 Ti on the exposed surface of the diffusion regions 1C
and 1D; and forming a silicide in a self-aligned
manner by causing a reaction between the metal layer
and the diffusion region. The remaining metal layer
may be removed by an etching process. See for example
20 the process disclosed in the Japanese Laid-Open Patent
Publication 7-115198.

In such a conventional process of forming a
silicide layer, however, there is a substantial risk
that the etching process, used in the step of FIG.1G
25 for removing the SiN film 4 from the bottom of the
contact holes 5A and 5B, may proceed further to the
diffusion region 1C or 1D and cause a damage thereto.

In order to be sure that such a damage is
not to be caused, it is necessary to deposit another
30 SiO₂ film in the step of FIG.1E before depositing the
SiN film 4, as an etching stopper. It should be noted
that the additional SiO₂ film acts as an etching
stopper for the etching process employed for removing
the SiN film 4, and the problem of damaging of the
35 diffusion region 1C or 1D is positively eliminated.
Further, such an additional SiO₂ film can be easily
removed by a selective etching process without causing

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1 a damage to the diffusion region 1C or 1D.

It is generally practiced to form such an
SiO₂ etching stopper layer by a CVD process. In the
case of the a semiconductor device in which the
5 silicide layer is formed on the surface of a shallow
diffusion region, however, there is a substantial risk
that the metal elements constituting the silicide may
cause a diffusion and reach the Si substrate because
of the high deposition temperature employed in the CVD
10 process. Thus, it has been necessary to form the
additional SiO₂ film by using a plasma CVD process at
a low temperature of typically about 500°C or less.

On the other hand, the SiO₂ etching stopper
film thus deposited at a low temperature plasma CVD
15 process tends to contain H₂O therein. As the SiO₂
etching stopper is covered by the SiN film 4 in the
step of FIG.1G, it is difficult for the H₂O molecules
in the SiO₂ etching stopper film to escape therefrom
once covered by the SiN film 4. Thereby, the H₂O
20 molecules tend to be confined in the SiO₂ film in the
form of OH and H ions. It should be noted that the OH
ions in the SiO₂ etching stopper film, when reached to
a region close to the gate oxide film 2 by way of
diffusion, may form a surface state which captures
25 electrons.

FIG.2 shows an example of the self-aligned
contact structure that uses an SiO₂ etching stopper
film, wherein those parts corresponding to the parts
described previously are designated by the same
30 reference numerals and the description thereof will be
omitted.

Referring to FIG.2, there is provided an
etching stopper film 6 of SiO₂ on the gate oxide film
2 by a low temperature plasma CVD process such that
35 the SiO₂ film 6 covers the gate electrode 3A including
the side wall oxide films 3a and 3b. Further, the SiN
film 4 is provided so as to cover the SiO₂ film 6.

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1 In such a structure, the escaping of H₂O
from the SiO₂ film 6 is difficult as already noted,
due to the existence of the SiN film 4 covering the
SiO₂ film 6. Thus, there is a substantial risk that
5 the OH ions confined in the SiO₂ film 6 cause a
diffusion toward the interface between the gate oxide
film 2 and the Si substrate 1. As noted already, the
OH ions thus reached the foregoing interface may form
a surface state that captures electrons, particularly
10 the hot electrons created in the channel region right
underneath the gate electrode 3A. The capturing of
the hot electrons by the surface state may in turn
cause an unwanted shift of threshold voltage of the
semiconductor device.

15 It should be noted that the self-aligned
contact structure of FIGS.1A - 1H may also be used in
a high-speed semiconductor memory device that has a
so-called local interconnection structure such as
SRAM. In the semiconductor device having such a local
20 interconnection structure, there tends to occur a
reaction between the metal layer forming the local
interconnection structure and a silicide that is
formed on the surface of the diffusion region. In
order to avoid the foregoing problem, it is necessary
25 to conduct the deposition of the etching stopper film
6 at a low temperature. However, such a low
temperature deposition of the SiO₂ etching stopper
film 6 causes the problem explained above.

30 SUMMARY OF THE INVENTION

Accordingly, it is a general object of the
present invention to provide a novel and useful
semiconductor device and a fabrication process thereof
wherein the foregoing problems are eliminated.

35 Another and more specific object of the
present invention is to provide a semiconductor device
having a self-aligned contact structure and a

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1 fabrication process thereof wherein the H₂O content in
the SiO₂ etching stopper film that is provided
underneath a nitride etching stopper film is minimized
without causing a diffusion of a metal element from
5 the silicide layer formed on a diffusion region to the
interior of the diffusion region, or without causing a
reaction between the silicide layer formed on the
surface of the diffusion region and a local
interconnection layer contacting the diffusion region.

10 Another object of the present invention is
to provide a method of fabricating a semiconductor
device, comprising the steps of:

forming a gate electrode on a substrate;
forming a diffusion region in said substrate
15 adjacent to said gate electrode;
forming a side wall oxide film on a side
wall of said gate electrode;
forming an interlayer insulation film on
said substrate such that said interlayer insulation
20 film covers said gate electrode and further said side
wall oxide film; and
forming a self-aligned opening in said
interlayer insulation film such that said self-aligned
opening exposes said diffusion region;
25 said step of forming said self-aligned
opening comprising the steps of:
forming a first insulation film of an oxide
such that said first insulation film covers said side
wall oxide film and said diffusion region;
30 depositing a second insulation film having a
composition different from a composition of said first
insulation film, on said first insulation film;
forming said interlayer insulation film on
said second insulation film;
35 forming a contact hole in said interlayer
insulation film in correspondence to said diffusion
region by an etching process while using said second

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1 insulation film as an etching stopper;
removing said second insulation film exposed
at a bottom of said contact hole by an etching process
while using said first insulation film as an etching
5 stopper; and
removing said first insulation film exposed
at a bottom of said contact hole selectively with
respect to said diffusion region;
wherein said step of forming said first
10 insulation film is conducted by a plasma CVD process,
with a high-frequency power set smaller than a high-
frequency power in which said first insulation film
contains H₂O with an amount of about 2.4 wt%.
Another object of the present invention is
15 to provide a semiconductor device, comprising:
a substrate;
a gate electrode provided on said substrate;
a diffusion region formed in said substrate
adjacent to said gate electrode;
20 a side-wall insulation film formed on a side
wall of said gate electrode; and
a self-aligned contact hole defined by said
side-wall oxide film and exposing said diffusion
region;
25 wherein said semiconductor device further
includes:
a first insulation film provided on said
gate electrode so as to cover said side wall oxide
film partially;
30 a second insulation film having a
composition different from a composition of said first
insulation film and provided on said first insulation
film;
an interlayer insulation film deposited on
35 said second insulation film;
a contact hole formed in said interlayer
insulation film, said contact hole extending through

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1 said first and second insulation films and exposing
said self-aligned contact hole;

 said first insulation film contains H₂O with
an amount smaller than about 2.4 wt%.

5 According to the present invention, the
formation of H₂O in the plasma is suppressed in the
low-power plasma CVD process used for forming the
first insulation film, by suppressing the high-
frequency plasma power. Thereby, the amount of H₂O
10 incorporated into the first insulation film is
successfully reduced below about 2.4 wt%, preferably
below about 1.1 wt%. As the first insulation film is
formed at a low temperature in the present invention,
the problem of thermal diffusion of the metal element
15 contained in the silicide layer covering the surface
of the diffusion region into the interior of the
diffusion region, is successfully avoided.

 Another object of the present invention is
to provide a method of fabricating a semiconductor
20 device, comprising the steps of:

 forming a gate electrode on a substrate;

 forming a diffusion region in said substrate
adjacent to said gate electrode;

 forming a side wall oxide film on a side
25 wall of said gate electrode;

 forming an interlayer insulation film on
said substrate such that said interlayer insulation
film covers said gate electrode and further said side
wall oxide film; and

30 forming a self-aligned opening in said
interlayer insulation film such that said self-aligned
opening exposes said diffusion region;

 said step of forming said self-aligned
opening comprising the steps of:

35 forming a first insulation film of an oxide
such that said first insulation film covers said side
wall oxide film and said diffusion region;

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- 1 depositing a second insulation film having a
composition different from a composition of said first
insulation film, on said first insulation film;
 forming said interlayer insulation film on
5 said second insulation film;
 forming a contact hole in said interlayer
insulation film in correspondence to said diffusion
region by an etching process while using said second
insulation film as an etching stopper;
10 removing said second insulation film exposed
at a bottom of said contact hole by an etching process
while using said first insulation film as an etching
stopper; and
 removing said first insulation film exposed
15 at a bottom of said contact hole selectively with
respect to said diffusion region;
 wherein said step of forming said first
insulation film is conducted by a CVD process that
uses SiH_4 and N_2O as source gases.
20 According to the present invention, the
proportion of the Si-H bond in the first insulation
film is increased when forming the first insulation
film by a plasma CVD process or a high-temperature CVD
process, by increasing the proportion of N_2O with
25 respect to SiH_4 . Thereby, the formation of H_2O in the
deposition chamber is successfully reduced and so is
the amount of H_2O in the first insulation film.
 Another object of the present invention is
to provide a method of fabricating a semiconductor
30 device, comprising the steps of:
 forming a gate electrode on a substrate;
 forming a diffusion region in said substrate
adjacent to said gate electrode;
 forming a side wall oxide film on a side
35 wall of said gate electrode;
 forming an interlayer insulation film on
said substrate such that said interlayer insulation

1 film covers said gate electrode and further said side
wall oxide film; and
forming a self-aligned opening in said
interlayer insulation film such that said self-aligned
5 opening exposes said diffusion region;
said step of forming said self-aligned
opening comprising the steps of:
forming a first insulation film of an oxide
such that said first insulation film covers said side
10 wall oxide film and said diffusion region;
depositing a second insulation film having a
composition different from a composition of said first
insulation film, on said first insulation film;
forming said interlayer insulation film on
15 said second insulation film;
forming a contact hole in said interlayer
insulation film in correspondence to said diffusion
region by an etching process while using said second
insulation film as an etching stopper;
20 removing said second insulation film exposed
at a bottom of said contact hole by an etching process
while using said first insulation film as an etching
stopper; and
removing said first insulation film exposed
25 at a bottom of said contact hole selectively with
respect to said diffusion region;
wherein said step of forming said first
insulation film is conducted by depositing a silicate
glass containing P.
30 Another object of the present invention is
to provide a semiconductor device, comprising:
a substrate;
a gate electrode provided on said substrate;
a diffusion region formed in said substrate
35 adjacent to said gate electrode;
a side-wall insulation film formed on a side
wall of said gate electrode; and

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1 a self-aligned contact hole defined by said
side-wall oxide film and exposing said diffusion
region;
 wherein said semiconductor device further
5 includes:
 a first insulation film provided on said
gate electrode so as to cover said side wall oxide
film partially;
 a second insulation film having a
10 composition different from a composition of said first
insulation film and provided on said first insulation
film;
 an interlayer insulation film deposited on
said second insulation film;
15 a contact hole formed in said interlayer
insulation film, said contact hole extending through
said first and second insulation films and exposing
said self-aligned contact hole;
 said first insulation film is formed of PSG
20 containing P with an amount of about 6 wt% or less.
 Another object of the present invention is
to provide a semiconductor device, comprising:
 a substrate;
 a gate electrode provided on said substrate;
25 a diffusion region formed in said substrate
adjacent to said gate electrode;
 a side-wall insulation film formed on a side
wall of said gate electrode; and
 a self-aligned contact hole defined by said
30 side-wall oxide film and exposing said diffusion
region;
 wherein said semiconductor device further
includes:
 a first insulation film provided on said
35 gate electrode so as to cover said side wall oxide
film partially;
 a second insulation film having a

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1 composition different from a composition of said first
insulation film and provided on said first insulation
film;

an interlayer insulation film deposited on
5 said second insulation film;

a contact hole formed in said interlayer
insulation film, said contact hole extending through
said first and second insulation films and exposing
said self-aligned contact hole;

10 said first insulation film is formed of BPSG
containing B with an amount of about 4 wt% or less.

According to the present invention, the
amount of H₂O in the first insulation film is
successfully reduced by the gettering action of P or B
15 that is contained in the PSG or BPSG forming the first
insulation film. Even when a high-temperature CVD
process is used for forming the first insulation film,
the problem of diffusion of the metal elements from
the silicide is successfully avoided by employing a
20 rapid heating process. Thereby, it is possible to
reduce the resistance of very shallow diffusion region
of a highly miniaturized high-speed semiconductor
device.

Other objects and further features of the
25 present invention will become apparent from the
following detailed description when read in
conjunction with the attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

30 FIGS.1A - 1H are diagrams showing a
conventional fabrication process of a semiconductor
device that has a self-aligned contact hole;

FIG.2 is a diagram showing the problem of a
conventional semiconductor device;

35 FIG.3 is a diagram showing the principle of
the present invention;

FIG.4 is another diagram showing the

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1 principle of the present invention;

FIG.5 is a still other diagram showing the principle of the present invention;

5 FIG.6 is a still other diagram showing the principle of the present invention;

FIG.7 is a still other diagram showing the principle of the present invention;

FIG.8 is a still other diagram showing the principle of the present invention;

10 FIG.9 is a still other diagram showing the principle of the present invention;

FIG.10 is a still other diagram showing the principle of the present invention;

15 FIG.11 is a still other diagram showing the principle of the present invention;

FIG.12 is a still other diagram showing the principle of the present invention;

FIG.13 is a still other diagram showing the principle of the present invention;

20 FIG.14 is a still other diagram showing the principle of the present invention;

FIGS.15A - 15I are diagrams showing the fabrication process of a semiconductor device according to a first embodiment of the present invention; and

25 FIGS.16A - 16O are diagrams showing the fabrication process of a semiconductor device according to a second embodiment of the present invention.

30

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS
[PRINCIPLE]

FIGS.3 - 14 are diagrams showing the content of H_2O incorporated into an SiO_2 film when the SiO_2 film is formed by a plasma CVD process, wherein FIGS.3
35 - 14 show the result obtained by a TDS (thermal desorption spectroscopy).

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1 Referring to the drawings, FIG.3 shows a
reference specimen in which the SiO_2 film is formed on
a Si substrate by a plasma CVD process conducted at a
substrate temperature of 480°C while setting the high-
5 frequency power to a conventional power of 200W.
FIG.4, on the other hand, shows a case in which the
 SiO_2 film is formed on a Si substrate at a substrate
temperature of 400°C while setting the high-frequency
power to 200W.

10 In the experiments, the plasma CVD process
is conducted in a parallel-plate-type plasma CVD
apparatus while supplying SiH_4 and N_2O as the gaseous
source materials, with a proportion set typically to
1:40. The TDS analysis, on the other hand, was
15 conducted by analyzing the chemical species,
particularly H_2O and OH, released from the SiO_2 film
as a result of the heating by a mass spectroscopy
while heating the substrate in the temperature range
illustrated in the drawings. In the drawings, it
20 should be noted that the horizontal axis represents
the duration in terms of minutes while the vertical
axis represents the partial pressure of the released
species in terms of Torr.

Referring to FIGS.3 and 4, it can be seen
25 that a substantial release of H_2O and OH occurs in the
 SiO_2 film deposited under a conventional plasma power
of 200°C immediately after the start of the heating.
The release of H_2O and OH continues even when the
temperature reaches 1000°C .

30 FIGS.5 and 6, on the other hand, show the
case in which the high-frequency power is set to 100W
and 50W respectively when depositing the SiO_2 film on
a Si substrate by a similar plasma CVD process.

Referring to FIGS.4 and 6, it is clearly
35 seen that the amount of H_2O and OH incorporated into
the SiO_2 film is reduced substantially by reducing the
high-frequency power used in the plasma CVD process.

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1 Further, FIG.7 shows the release of H_2O and
OH from the SiO_2 film deposited on the Si substrate at
a substrate temperature of $400^\circ C$ and a plasma power of
100W for a case in which the ratio of N_2O with respect
5 to H_2O in the gaseous source is set to 10. In this
case, the SiO_2 film obtained as a result of the plasma
CVD process has a refractive index of about 1.5. In
contrast, it should be noted that the SiO_2 film
obtained in FIG.5 has a refractive index of about
10 1.47. Further, the SiO_2 film of FIG.3 shows a
refractive index of about 1.45.

As can be seen in FIG.7, the amount of H_2O
and OH incorporated into the SiO_2 film is reduced
further as compared with the case of FIG.5. It is
15 believed that the foregoing decrease of H_2 and OH
content in the SiO_2 film observed in the case of FIG.7
is caused by the increased amount of Si-H bond in the
 SiO_2 film.

When the proportion of N_2O with respect to
20 SiH_4 is increased further as in the case of FIG.8, on
the other hand, the amount of H_2O and OH incorporated
into the SiO_2 film starts to increase again. Thus, it
is concluded that the plasma CVD process for
depositing an SiO_2 film is preferably conducted such
25 that the deposited SiO_2 film has a refractive index of
higher than about 1.5 but lower than about 1.63.

FIG.9 shows a differential in which the
result of FIG.3 is subtracted from the result of
FIG.5. As already explained with reference to FIG.4,
30 the SO_2 film deposited under the plasma power of 200W
contains a large amount of H_2O and OH.

FIG.10 shows, on the other hand, a
differential in which the result of FIG.3 is
subtracted from the result of FIG.5 in which the high-
35 frequency power is set to 100W. As can be seen
clearly from FIG.10, the amount of H_2O and OH released
from the SiO_2 film deposited under the high-frequency

09045118-032058

1 power of 100W is reduced substantially.

Further, FIG.11 shows a differential in
which the result of FIG.3 is subtracted from the
result of FIG.6 in which the high-frequency power is
5 set to 50W. As can be seen clearly from FIG.10, the
amount of H_2O and OH released from the SiO_2 film
deposited under the high-frequency power of 50W is
reduced further as compared with the case of FIG.10.

Further, FIG.12 shows a differential in
10 which the result of FIG.3 is subtracted from the
result of FIG.7 in which the deposited SiO_2 film has a
refractive index of 1.5. In this case, the amount of
release of H_2O and OH is reduced further. In
contrast, FIG.13 shows the case in which the result of
15 FIG.3 is subtracted from the result of FIG.10 in which
the deposited SiO_2 film has a refractive index of
1.63. In this case, the amount of H_2O and OH
incorporated into the SiO_2 film starts to increase
again.

20 Summarizing above, it is possible to
minimize the amount of H_2O and OH incorporated into
the underlying insulation film 6 of the semiconductor
structure of FIG.2, by setting the high-frequency
power, used for a plasma formation, to about 100W or
25 less when depositing the insulation film 6 by a plasma
CVD process, or alternatively by setting the ratio of
 SiH_4 and N_2O in a gaseous source material such that
the insulation film 6 has a refractive index of about
1.5.

30 The amount of H_2O and OH incorporated into
the insulation film 6 of FIG.2 can be minimized also
by incorporating P or B into the film 6. In this
case, therefore, the insulation film 6 has a
composition of PSG or BPSG.

35 FIG.14 shows the penetration of D_2O into a
PSG or BPSG film for a case in which the PSG or BPSG
film is exposed to a vapor moisture (Pramanik, D.,

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1 Solid State Technology, September 1995, pp.69-78).

Referring to FIG.14, it can be seen that the amount of OH penetrating into a PSG or BPSG film decreases when the P or B content in the film is increased. It is believed that the P or B ions incorporated into the PSG or BPSG film perform a gettering action of H₂O therein. When such a PSG or BPSG film is to be used for the insulation film 6 of FIG.2, it is preferable to set the amount of P to about 6 wt% or less and the amount of B to about 4 wt% or less.

In the structure of FIG.2, it should be noted that the insulation film 6 may be formed by an ordinary high-temperature CVD process when the substrate temperature is held below about 800°C. In such a case, too, it is desirable to increase the proportion of Si-H bond in the film by increasing the ratio of SiH₄ with respect to N₂O similarly to the case of the plasma CVD process described before. An SiO₂ film containing a large amount of Si-H bond tends to show a high refractive index. Further, it is also possible to apply a thermal annealing process to the oxide film 6 prior to the deposition of the SiN film 4 and cause a releasing of H₂O. By using a rapid thermal annealing process, it is possible to minimize the unwanted thermal effect on the silicide layer covering the diffusion region.

[FIRST EMBODIMENT]

30 FIGS.15A - 15I show a fabrication process of a MOS transistor according to a first embodiment of the present invention.

Referring to FIG.15A, a gate oxide film 12 and a field oxide film 12A are formed on a p-type Si substrate 11 corresponding to the Si substrate 1 of FIG.1A, and a polysilicon layer 13 is deposited on the structure of FIG.15A in the step of FIG.15B. The

1 polysilicon layer 13 thus deposited is then doped to
the n^+ -type by an ion-implantation of P^+ ions and
patterned in the step of FIG.15C to form a gate
electrode 13A. The ion implantation process of
5 FIG.15B may be conducted under an acceleration voltage
of 20 keV with a dose of $4 \times 10^{15} \text{cm}^{-2}$. In the step of
FIG.15C, an ion implantation process of As^+ is further
conducted while using the gate electrode 13A as a
mask, to form shallow diffusion regions 11A and 11B of
10 the n^+ -type at both lateral sides of the gate
electrode 13A by a self-alignment process. The ion
implantation process of FIG.15C may be conducted under
an acceleration voltage of 10 keV with a dose of $3 \times 10^{14} \text{cm}^{-2}$.

15 Next, in the step of FIG.15D, an SiO_2 film
is deposited on the structure of FIG.15C uniformly by
a CVD process, followed by an anisotropic etching
process acting substantially perpendicularly to the
surface of the substrate 11 to form side wall oxide
20 films 13a and 13b on both side walls of the gate
electrode 13A. Further, additional diffusion regions
11C and 11D are formed so as to partially overlap the
diffusion region 11A or 11B by conducting an ion-
implantation process of As^+ while using the gate
25 electrode 13A and the side-wall oxide films 13a and
13b as a mask, to form a so-called LDD (lightly doped
drain) structure. The ion implantation process of
FIG.15D may be conducted under an acceleration voltage
to 40 keV with a dose of $2 \times 10^{15} \text{cm}^{-2}$.

30 Next, in the step of FIG.15E, those parts of
the gate oxide film 12 covering the diffusion regions
11C and 11D are removed and a Co layer (not shown) is
deposited in contact with the exposed diffusion
regions and further on the gate electrode 13A.
35 Further, by applying a thermal annealing process
conducted at 840°C for about 30 seconds, the Co layer
thus deposited causes a reaction with the exposed

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1 surface of the diffusion regions 11C and 11D as well
as the gate electrode 13A, and there are formed a
silicide film 11E on the surface of the diffusion
region 11C as indicated in FIG.15E. Similarly, a
5 silicide film 11F is formed on the surface of the
diffusion region 11D and a silicide film 13B is formed
on the gate electrode 13A.

Next, in the step of FIG.15F, an SiO_2 film
14 is deposited on the structure of FIG.15E by a
10 plasma CVD process with a thickness of about 20 nm.
Thereby, the deposition of the SiO_2 film 14 is
conducted in a parallel-plate-type plasma CVD
apparatus under a pressure of 3.0 Torr while setting
the substrate temperature to 400°C and the high-
15 frequency power to 50 kW. During the deposition of
the SiO_2 film 14, SiH_4 and N_2O are supplied to the
reaction chamber of the plasma CVD apparatus as source
materials together with an N_2 carrier gas with a flow
rate of 10cc/min and 400cc/min respectively. The flow
20 rate of the N_2 carrier gas may be set to 2000 cc/min.
The plasma CVD apparatus may have an electrode gap of
300 Mil.

It should be noted that the SiO_2 film 14
thus deposited contains H_2O with an amount of about
25 1.1 wt% or less due to the decreased H_2O formation in
the plasma, wherein the foregoing amount of H_2O in the
film 14 is substantially smaller than the H_2O content
of the SiO_2 film of FIG.3 of about 2.4 wt%. Further,
it should be noted that the SiO_2 film 14 thus formed
30 has a refractive index of about 1.47.

The evaluation of the H_2O content in the
 SiO_2 film 14 is achieved by first calculating the
total number of the H_2O molecules (Mm) released from
the SiO_2 film as a result of the TDS analysis from the
35 time-integral of the partial pressure value (Pxt) of
the released H_2O molecules according to the equation

1 $Mm = C \times ((Pxt)/S) \times 3.35 \times 10^{19},$

5 followed by dividing the value Mm by the weight of the
SiO₂ film 14, which in turn is obtained from the
volume of the SiO₂ film and the density thereof,
wherein the volume of the SiO₂ film is obtained from
the surface area of the substrate and the film
thickness. Further, it should be noted that the
10 parameter C of the foregoing equation stands for the
conductance of the orifice used in the TDS analysis
while the parameter S stands for the relative
sensitivity of the mass spectrometer used in the TDS
analysis. Further, the last numerical constant is for
15 the conversion of the obtained pressure integral value
to the corresponding molecule number by using an ideal
gas model. In the present case, the orifice
conductance C has a value of 27.5 l/sec, while the
relative sensitivity S has a value of 1 for H₂O.

20 Next, in the step of FIG.15G, an SiN film 15
is deposited uniformly on the structure of FIG.15F by
a CVD process or a sputtering process, followed by the
step of FIG.15H in which an interlayer insulation film
16 of SiO₂, PSG or BPSG is deposited on the foregoing
25 SiN film 15. The interlayer insulation film 16 is
further formed with a contact hole 16A in
correspondence to the diffusion region 11C by an
anisotropic dry etching process. Similarly, a contact
hole 16B is formed in the insulation film 16 in
30 correspondence to the diffusion region 11D.

Further, in the step of FIG.15I, conductive
plugs 17A and 17B of polysilicon are provided so as to
fill the contact holes 16A and 16B respectively, and
an interconnection pattern 17 is provided on the
35 interlayer insulation film 16 in contact with the
conductive plug 17A or 17B.

According to the present embodiment, the H₂O

1 formation in the plasma is effectively suppressed by
conducting the plasma deposition of the oxide film 14
underneath the SiN film 15 by a reduced plasma power,
and the H₂O content incorporated into the SiO₂ film 14
5 is reduced accordingly. As the formation of the oxide
film 14 is conducted at a low temperature as a result
of use of the plasma CVD process, the problem of Co
diffusion and associated short-circuit of the
diffusion region, is effectively avoided even when the
10 step of formation of the oxide film 14 is conducted.

It should be noted that the formation of the
oxide film 14 may be conducted by setting the high-
frequency power to 100W. In this case, too, the same
parallel-plate-type plasma CVD apparatus is used and
15 the deposition is conducted at a substrate temperature
of about 400°C under an internal pressure of 3.0 Torr.
During the deposition, SiH₄ and N₂O are supplied as
the gaseous source respectively with a flow rate of 10
cc/min and a flow rate of 100 cc/min, together with an
20 N₂ carrier gas which is supplied to the reaction
chamber of the plasma CVD apparatus with a flow rate
of 2000 cc/min. The oxide film 14 thus formed has a
refractive index of about 1.5.

Further, it is possible to replace the SiO₂
25 film 14 by a PSG or BPSG film that contains P or B.
As noted already, P or B shows a gettering action of
H₂O. When a PSG film is to be used for the insulation
film 14, it is preferable to set the P content in the
PSG film 14 to be about 6 wt% or less. When a BPSG
30 film is to be used for the insulation film 14, on the
other hand, it is preferable to set the B content in
the film 14 to be about 4 wt% or less.

Further, it should be noted that the
foregoing oxide film 14 may be formed also by an
35 ordinary high-temperature CVD process. In this case,
it is preferable to set the substrate temperature to
about 825°C or less for minimizing the diffusion of

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1 metal elements from the silicide film and set the
ratio of N_2O with respect to SiH_4 to be less than
about 5 so as to maximize the Si-H bond formation in
the film. Further, it is also possible to cause a
5 release of H_2O from the oxide film 14 by applying a
thermal annealing process to the film 14 at a
temperature of about $825^{\circ}C$ prior to the deposition of
the SiN film 15.

As the deposition of the oxide film 14 and
10 the deposition of the SiN film 15 are conducted in the
same deposition apparatus continuously, the chance
that the deposited oxide film 14 contacts the
atmospheric environment and absorbs the moisture in
the atmosphere is positively eliminated.

15

[SECOND EMBODIMENT]

FIGS.16A - 160 show a fabrication process of
a semiconductor device according to a second
embodiment of the present invention.

20 Referring to FIG.16A, a Si substrate 21 of
the p-type or n-type is covered by a native oxide film
22N, and an SiN mask 23A as well as an SiN mask 23B are
provided on the substrate 21 such that the SiN mask
23A protects an NMOS region on which an NMOS
25 transistor is to be formed. Similarly, the SiN mask
23B protects a PMOS region on which a PMOS transistor
is to be formed. The mask 23A and 23B are separated
and there is formed a gap between the region for the
NMOS transistor and the region for the PMOS
30 transistor. The gap exposes the native oxide film 22N
formed on the substrate 21.

Next, in the step of FIG.16B, the structure
of FIG.16A is subjected to a wet oxidation process to
form a field oxide film 23 in correspondence to the
35 foregoing gap typically with a thickness of about 250
nm. Further, a mask M1 is provided in the step of
FIG.16B so as to cover the PMOS region, and an ion

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1 implantation of B^+ is conducted into the substrate 21
with an acceleration voltage of 300 keV and a dose of
3 x 10^{13}cm^{-2} . As a result of the ion implantation
process, a p-type well 21A is formed in the substrate
5 21 in a first side of the field oxide film 23 in
correspondence to the NMOS region.

Next, in the step of FIG.16C, the NMOS
region is covered by a mask M2 and an ion implantation
of P^+ is conducted into the substrate 21 with an
10 acceleration voltage of 600 keV and a dose of 3 x
 10^{13}cm^{-2} . As a result of the ion implantation
process, an n-type well 21B is formed in the substrate
21 in a second, opposite side of the field oxide film
23 in correspondence to the PMOS region.

15 Next, in the step of FIG.16D, the native
oxide film 22N is removed by an etching process and a
thermal oxide film 22 is formed on the surface of the
substrate 21 by a thermal oxidation process with a
thickness of about 5.5 nm. Further, a polysilicon
20 film 24 is formed in the step of FIG.16D on the
structure thus formed with a thickness of about 180
nm.

Next, in the step of FIG.16E, an oxide film
25 is formed on the structure of FIG.16D by an
25 ordinary high-temperature CVD process typically with a
thickness of 80 nm, and an opening 25A is formed in
the oxide film 25 thus formed in correspondence to a
part thereof covering the field oxide film 23 by using
a mask M3.

30 Next, in the step of FIG.16F, an SiN film 26
is formed on the oxide film 25 by a plasma CVD process
with a thickness of typically 26 nm. The SiN film 26
thus formed is patterned according to a desired gate
pattern by using a mask M4, and the oxide film 25 and
35 the polysilicon film 24 underneath the SiN film 26 are
patterned while using the SiN pattern 26 thus obtained
as a mask. Thereby, gate electrodes 24A - 24E are

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1 formed. It should be noted that the gate electrodes
24A and 24B thus formed are located on the well 21A,
while the gate electrodes 24C and 24D are formed on
the well 21B. Further, the gate electrode 24E is
5 formed on the field oxide film 23. Further, the oxide
films 22 exposed at both sides of the foregoing gate
electrodes are removed selectively.

Next, in the step of FIG.16G, the PMOS
region is protected by a mask M5, and an ion
10 implantation of As^+ is conducted into the gate
electrodes 24A and 24B under an acceleration voltage
of 10 keV with a dose of $3 \times 10^{14} \text{cm}^{-2}$. As a result of
the foregoing ion implantation process of As^+ ,
diffusion regions $21A_1$, $21A_2$ and $21A_3$ are formed in
15 the well 21A adjacent to the gate electrodes 24A and
24B.

Next, in the step of FIG.16H, each of the
gate electrodes 24A - 24E is formed with a pair of
side wall oxide films 24a and 24b by a well known
20 process that includes a CVD deposition of an oxide
film and an etch-back process. Further, the SiN film
25 is removed and the step of FIG.16I is conducted, in
which an ion implantation of As^+ is conducted into the
well 21A while using the gate electrodes 24A and 24B
and further the side wall oxide films 24a and 24b as a
mask, to form a diffusion region $21A_4$ in superposition
to the diffusion region $21A_1$ and a diffusion region
 $21A_5$ in superposition to the diffusion region $21A_2$.
Thereby, an LDD structure is formed in the well 21A in
30 the step of FIG.16I. It should be noted that the ion
implantation process of As^+ of FIG.16I is conducted
under an acceleration voltage of 40 keV with a dose of
 $2 \times 10^{15} \text{cm}^{-2}$, while protecting the PMOS region by a
mask M6.

35 Next, in the step of FIG.16J, the NMOS
region is protected by a mask M7, and an ion
implantation process of B^+ is conducted into the well

1 21B while using the gate electrodes 24C and 24D and
further the side wall oxide films 24a and 24b as a
mask. The ion implantation of B^+ is typically
conducted under an acceleration voltage of 7 keV with
5 a dose of $2 \times 10^{15} \text{cm}^{-2}$, and diffusion regions 21B₁,
21B₂ and 21B₃ are formed in the well 21B as a result.

Further, in the step of FIG.16K, the side
wall oxide films 24a and 24b on the gate electrodes
24A - 24E are grown laterally by depositing a CVD
10 oxide film further thereon, followed by an etch-back
process. In this process, the diffusion regions 21A₄
- 21A₆ as well as the diffusion regions 21B₁ - 21B₆
are exposed on the Si substrate 21, and a step of
FIG.16L is conducted in which a Co film (not shown) is
15 deposited by a sputtering process. It should be noted
that the diffusion regions 21A₄ - 21A₆ include therein
diffusion regions 21A₁ - 21A₃ respectively.

The structure thus obtained is then
subjected to a thermal annealing process conducted at
20 550°C for 30 minutes, to form a self-aligned silicide
(CoSi₂) layer 27 on the exposed surface of the
diffusion region. After the formation of the silicide
layer 27, the remaining Co layer is removed by an
etching process, and the overall structure is
25 subjected to a thermal annealing process conducted at
825°C for 20 seconds. It should be noted that the
silicide layer 27 is formed also on the exposed part
of the electrode 24E corresponding to the opening 25A.
See FIG.16E.

30 Next, in the step of FIG.16M, a TiN layer is
deposited on the structure of FIG.16L by a reactive
sputtering process typically with a thickness of about
20 nm, and the TiN layer thus deposited is patterned
subsequently while using a mask M8 to form local
35 interconnection patterns 28A, 28B and 28C in
electrical contact with the foregoing silicide layer
27. In the illustrated example, the diffusion regions

1 21A₃ and 21A₆ are formed in electrical connection with
the electrode 24E via the foregoing local
interconnection pattern 28B and the silicide layer 27,
and the semiconductor device forms an SRAM.

5 Next, in the step of FIG.16N, an oxide
(SiO₂) film 29 is formed on the structure of FIG.16M
by a plasma CVD process similarly to the oxide film 14
of the previous embodiment, with a thickness of 20 nm.

Thus, the deposition of the oxide film 29 is
10 conducted in a parallel-plate-type plasma CVD
apparatus at a substrate temperature of 400°C while
setting the high-frequency power to 50 kW. During the
deposition of the oxide film 29, the internal pressure
of the reaction chamber of the plasma CVD apparatus is
15 set to 3.0 Torr and SiH₄ and N₂O are supplied as the
gaseous source together with an N₂ carrier gas with
respective flow rates of 10 cc/min and 400 cc/min.
The flow rate of the N₂ carrier gas is set to about
2000 cc/min. Similarly as before, the gap between the
20 electrodes of the plasma CVD apparatus is set to 300
Mil. As the formation of H₂O in the plasma is
suppressed in the plasma CVD process conducted under
the foregoing conduction, the SiO₂ film 29 thus
obtained typically has an H₂O content of 1.1 wt% or
25 less and a refractive index of about 1.47.

After the foregoing formation of the oxide
film 29, an SiN film 30 is formed on the oxide film
29 by a plasma CVD process as indicated in FIG.16N
with a thickness of about 70 nm. Further, an
30 interlayer insulation film 31 of SOG or the like is
deposited on the structure of FIG.16N in the step of
FIG.16O.

It should be noted that the formation of the
oxide film 29 may be conducted by setting the high-
35 frequency power to 100W. In this case, too, the same
parallel-plate-type plasma CVD apparatus is used and
the deposition is conducted at a substrate temperature

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1 of about 400°C under an internal pressure of 3.0 Torr.
During the deposition, SiH_4 and N_2O are supplied as
the gaseous source respectively with a flow rate of 10
cc/min and a flow rate of 100 cc/min, together with an
5 N_2 carrier gas which is supplied to the reaction
chamber of the plasma CVD apparatus with a flow rate
of 2000 cc/min. The oxide film 29 thus formed has a
refractive index of about 1.5.

Further, it is possible to replace the SiO_2
10 film 29 by a PSG or BPSG film that contains P or B.
As noted already, P or B shows a gettering action of
 H_2O . When a PSG film is to be used for the insulation
film 29, it is preferable to set the P content in the
PSG film 29 to be about 6 wt% or less. When a BPSG
15 film is to be used for the insulation film 29, on the
other hand, it is preferable to set the B content in
the film 29 to be about 4 wt% or less.

Further, it should be noted that the
foregoing oxide film 29 may be formed also by an
20 ordinary high-temperature CVD process. In this case,
it is preferable to set the substrate temperature to
about 825°C or less for minimizing the diffusion of
metal elements from the silicide film and set the
ratio of N_2O with respect to SiH_4 to be less than
25 about 5 so as to maximize the Si-H bond formation in
the film. Further, it is also possible to cause a
release of H_2O from the oxide film 29 by applying a
thermal annealing process to the film 29 at a
temperature of about 825°C prior to the deposition of
30 the SiN film 30.

As the deposition of the oxide film 29 and
the deposition of the SiN film 30 are conducted in the
same deposition apparatus continuously, the chance
that the deposited oxide film 29 contacts the
35 atmospheric environment and absorbs the moisture in
the atmosphere is positively eliminated.

Further, the present invention is not

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1 limited to the embodiments described heretofore, but
various variations and modifications may be made
without departing from the scope of the present
invention.

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1 WHAT IS CLAIMED IS

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1. A method of fabricating a semiconductor device, comprising the steps of:

forming a gate electrode on a substrate;

10 forming a diffusion region in said substrate adjacent to said gate electrode;

forming a side wall oxide film on a side wall of said gate electrode;

15 forming an interlayer insulation film on said substrate such that said interlayer insulation film covers said gate electrode and further said side wall oxide film; and

forming a self-aligned opening in said interlayer insulation film such that said self-aligned opening exposes said diffusion region;

20 said step of forming said self-aligned opening comprising the steps of:

forming a first insulation film of an oxide such that said first insulation film covers said side wall oxide film and said diffusion region;

25 depositing a second insulation film having a composition different from a composition of said first insulation film, on said first insulation film;

forming said interlayer insulation film on said second insulation film;

30 forming a contact hole in said interlayer insulation film in correspondence to said diffusion region by an etching process while using said second insulation film as an etching stopper;

35 removing said second insulation film exposed at a bottom of said contact hole by an etching process while using said first insulation film as an etching stopper; and

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wherein said step of forming said first
5 insulation film is conducted by a plasma CVD process,
with a high-frequency power set smaller than a high-
frequency power in which said first insulation film
contains H₂O with an amount of about 2.4 wt%.

2. A method as claimed in claim 1, wherein
said high-frequency power is set smaller than a high-
15 frequency power in which said first insulation film
contains H₂O with an about of about 1.1 wt% or less.

3. A method as claimed in claim 1, wherein said high-frequency power is set smaller than about 100 W.

4. A method as claimed in claim 1, wherein said high-frequency power is set between about 50 W and about 100 W.

35 5. A method as claimed in claim 1, wherein
said first insulation film has a refractive index of
about 1.5.

1 6. A method as claimed in claim 1, wherein
said plasma CVD process is conducted while using SiH_4
and N_2O as source materials, with a proportion of N_2O
with respect to SiH_4 set to be about 10 or less.

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10 7. A method as claimed in claim 1, further
including a step, after said step of forming said
first insulation film and before said step of forming
said second insulation film, of annealing said first
insulation film.

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20 8. A method as claimed in claim 7, wherein
said annealing step is conducted by a rapid heating
process.

25 9. A method as claimed in claim 1, wherein
said step of forming said first insulation film and
said step of forming said second insulation film are
conducted in a common reaction vessel, without a step
of taking out said substrate outside said reaction
30 vessel.

35 10. A method as claimed in claim 1,
wherein said step of forming said diffusion region
includes a step of forming a silicide on a surface of

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1 said diffusion region, and wherein said step of
forming said silicide is conducted before said step of
forming said first insulation film.

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11. A method as claimed in claim 1, further
comprising a step, before said step of forming said
10 first insulation layer, of forming a conductor pattern
in contact with said diffusion region.

15

12. A method of fabricating a semiconductor
device, comprising the steps of:
forming a gate electrode on a substrate;
forming a diffusion region in said substrate
20 adjacent to said gate electrode;
forming a side wall oxide film on a side
wall of said gate electrode;
forming an interlayer insulation film on
said substrate such that said interlayer insulation
25 film covers said gate electrode and further said side
wall oxide film; and
forming a self-aligned opening in said
interlayer insulation film such that said self-aligned
opening exposes said diffusion region;
30 said step of forming said self-aligned
opening comprising the steps of:
forming a first insulation film of an oxide
such that said first insulation film covers said side
wall oxide film and said diffusion region;
35 depositing a second insulation film having a
composition different from a composition of said first
insulation film, on said first insulation film;

03045149-030090

1 forming said interlayer insulation film on
said second insulation film;
 forming a contact hole in said interlayer
insulation film in correspondence to said diffusion
5 region by an etching process while using said second
insulation film as an etching stopper;
 removing said second insulation film exposed
at a bottom of said contact hole by an etching process
while using said first insulation film as an etching
10 stopper; and
 removing said first insulation film exposed
at a bottom of said contact hole selectively with
respect to said diffusion region;
 wherein said step of forming said first
15 insulation film is conducted by a CVD process that
uses SiH_4 and N_2O as source gases.

20 13. A method as claimed in claim 12,
wherein said CVD process is conducted while setting a
ratio of N_2O with respect to SiH_4 to about 5 or less.

25 14. A method as claimed in claim 12,
wherein said CVD process is conducted at a substrate
30 temperature of about 825°C or less.

35 15. A method as claimed in claim 12,
further including a step, after said step of forming
said first insulation film and before said step of

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1 forming said second insulation film, of annealing said
first insulation film.

5

16. A method as claimed in claim 12,
wherein said annealing step is conducted by a rapid
heating process.

10

17. A method as claimed in claim 12,
15 wherein said step of forming said first insulation
film and said step of forming said second insulation
film are conducted in a common reaction vessel,
without a step of taking out said substrate outside
said reaction vessel.

20

18. A method as claimed in claim 12,
25 wherein said step of forming said diffusion region
includes a step of forming a silicide on a surface of
said diffusion region, and wherein said step of
forming said silicide is conducted before said step of
forming said first insulation film.

30

19. A method of fabricating a semiconductor
35 device, comprising the steps of:

forming a gate electrode on a substrate;
forming a diffusion region in said substrate

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1 adjacent to said gate electrode;
forming a side wall oxide film on a side
wall of said gate electrode;
forming an interlayer insulation film on
5 said substrate such that said interlayer insulation
film covers said gate electrode and further said side
wall oxide film; and
forming a self-aligned opening in said
interlayer insulation film such that said self-aligned
10 opening exposes said diffusion region;
said step of forming said self-aligned
opening comprising the steps of:
forming a first insulation film of an oxide
such that said first insulation film covers said side
15 wall oxide film and said diffusion region;
depositing a second insulation film having a
composition different from a composition of said first
insulation film, on said first insulation film;
forming said interlayer insulation film on
20 said second insulation film;
forming a contact hole in said interlayer
insulation film in correspondence to said diffusion
region by an etching process while using said second
insulation film as an etching stopper;
25 removing said second insulation film exposed
at a bottom of said contact hole by an etching process
while using said first insulation film as an etching
stopper; and
removing said first insulation film exposed
30 at a bottom of said contact hole selectively with
respect to said diffusion region;
wherein said step of forming said first
insulation film is conducted by depositing a silicate
glass containing P.

35

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1 20. A method as claimed in claim 19,
wherein said silicate glass contains P therein with an
amount of about 6 wt% or less.

5

 21. A method as claimed in claim 19,
wherein said silicate glass further contains B.
10

 22. A method as claimed in claim 21,
15 wherein said silicate glass contains B with an amount
of about 4 wt% or less.

20

 23. A method as claimed in claim 19,
further including a step, after said step of forming
said first insulation film and before said step of
forming said second insulation film, of annealing said
25 first insulation film.

30 24. A method as claimed in claim 23,
wherein said annealing step is conducted by a rapid
heating process.

35

 25. A method as claimed in claim 19,

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1 wherein said step of forming said first insulation
film and said step of forming said second insulation
film are conducted in a common reaction vessel,
without a step of taking out said substrate outside
5 said reaction vessel.

10 26. A method as claimed in claim 19,
wherein said step of forming said diffusion region
includes a step of forming a silicide on a surface of
said diffusion region, and wherein said step of
forming said silicide is conducted before said step of
15 forming said first insulation film.

20 27. A method as claimed in claim 19,
further comprising a step, before said step of forming
said first insulation layer, of forming a conductor
pattern in contact with said diffusion region.

25

28. A semiconductor device, comprising:
a substrate;
30 a gate electrode provided on said substrate;
a diffusion region formed in said substrate
adjacent to said gate electrode;
a side-wall insulation film formed on a side
wall of said gate electrode; and
35 a self-aligned contact hole defined by said
side-wall oxide film and exposing said diffusion
region;

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1 wherein said semiconductor device further
includes:

 a first insulation film provided on said
gate electrode so as to cover said side wall oxide
5 film partially;

 a second insulation film having a
composition different from a composition of said first
insulation film and provided on said first insulation
film;

10 an interlayer insulation film deposited on
said second insulation film;

 a contact hole formed in said interlayer
insulation film, said contact hole extending through
said first and second insulation films and exposing
15 said self-aligned contact hole;

 said first insulation film contains H₂O with
an amount smaller than about 2.4 wt%.

20

 29. A semiconductor device as claimed in
claim 28, wherein said first insulation film contains
H₂O with an amount of about 1.1 wt% or less.

25

 30. A semiconductor device as claimed in
30 claim 28, wherein said first insulation film is an
oxide film having a refractive index of about 1.5.

35

 31. A semiconductor device as claimed in
claim 28, further comprising a conductor pattern

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10 32. A semiconductor device as claimed in
claim 28, further comprising a silicide layer on a
surface of said diffusion region.

15

33. A semiconductor device as claimed in claim 32, further comprising a silicide layer on a surface of said gate electrode.

34. A semiconductor device, comprising:

25 a substrate;

a gate electrode provided on said substrate;

a diffusion region formed in said substrate

adjacent to said gate electrode;

a side-wall insulation film formed on a side

30 wall of said gate electrode; and

a self-aligned contact hole defined by said

side-wall oxide film and exposing said diffusion

region;

wherein said semiconductor device further

35 includes:

a first insulation film provided on said

gate electrode so as to cover said side wall oxide

1 film partially;
a second insulation film having a
composition different from a composition of said first
insulation film and provided on said first insulation
5 film;
an interlayer insulation film deposited on
said second insulation film;
a contact hole formed in said interlayer
insulation film, said contact hole extending through
10 said first and second insulation films and exposing
said self-aligned contact hole;
said first insulation film is formed of PSG
containing P with an amount of about 6 wt% or less.

15

35. A semiconductor device as claimed in
claim 34, further comprising a conductor pattern
20 contacting with said diffusion region and said gate
electrode such that said conductor pattern extends
between said side wall oxide film and said first
insulation film along a surface of said side wall
oxide film.

25

36. A semiconductor device as claimed in
claim 34, further comprising a silicide layer on a
30 surface of said diffusion region.

35

38. A semiconductor device as claimed in
claim 36, further comprising a silicide layer on a

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5

a substrate;

a diffusion region formed in said substrate

a side-wall insulation film formed on a side wall of said gate electrode; and

a self-aligned contact hole defined by said side-wall oxide film and exposing said diffusion

wherein said semiconductor device further

a first insulation film provided on said gate electrode so as to cover said side wall oxide

a second insulation film having a

an interlayer insulation film deposited on
said second insulation film;

a contact hole formed in said interlayer insulation film, said contact hole extending through said first and second insulation films and exposing

said first insulation film is formed of BPSG

40. A semiconductor device as claimed in

1 claim 39, further comprising a conductor pattern
contacting with said diffusion region and said gate
electrode such that said conductor pattern extends
between said side wall oxide film and said first
5 insulation film along a surface of said side wall
oxide film.

10

41. A semiconductor device as claimed in
claim 39, further comprising a silicide layer on a
surface of said diffusion region.

15

42. A semiconductor device as claimed in
claim 41, further comprising a silicide layer on a
20 surface of said gate electrode.

25

30

35

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1 ABSTRACT OF THE DISCLOSURE

 A semiconductor device having a self-aligned
contact hole is formed by providing a side wall oxide
film on a gate electrode, covering the gate electrode
5 and the side wall oxide film by an oxide film and
further covering the oxide film by a nitride film,
wherein the oxide film is formed by a plasma CVD
process with a reduced plasma power such that the H₂O
content in the oxide film is less than about 2.4 wt%.

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15

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Declaration For U.S. Patent Application

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
(Insert Title) SEMICONDUCTOR DEVICE HAVING A SELF-ALIGNED CONTACT HOLE

the specification of which is attached hereto unless the following is checked:

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 (a) - (d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

(List prior foreign applications. See note A on back of this page)	Pat. Appln. <u>No. 9-191239</u> (Number)	<u>Japan</u> (Country)	<u>16/July/1997</u> (Day/Month/Year Filed)	Priority Claimed <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
	(Number)	(Country)	(Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No
	(Number)	(Country)	(Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No
	(Number)	(Country)	(Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No
	(Number)	(Country)	(Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No

See note B on back of this page ☐ See attached list for additional prior foreign applications

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of the application:

(List Prior U.S. Applications)	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)
	(Application Serial Number)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

James E. Armstrong, III, Reg. No. 18,366; William F. Westerman, Reg. No. 29,988; Ken-Ichi Hattori, Reg. No. 32,861; Le-Nhung McLeland, Reg. No. 31,541; Ronald F. Naughton, Reg. No. 24,616; John R. Pegan, Reg. No. 18,069; William G. Kratz, Jr., Reg. No. 22,631; Albert Tockman, Reg. No. 19,722; Mel R. Quintos, Reg. No. 31,898; Donald W. Hanson, Reg. No. 27,133; Stephen G. Adrian, Reg. No. 32,878; William L. Brooks, Reg. No. 34,129; John F. Carney, Reg. No. 20,276; Edward F. Welsh, Reg. No. 22,455; Patrick D. Muir, Reg. No. 37,403; Gay A. Spahn, Reg. No. 34,978; and John P. Kong, Reg. No. 40,054.

ect all communications to the following address:

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McLELAND & NAUGHTON
1725 K Street, N.W., Suite 1000
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Telephone: (202) 659-2930 Fax: (202) 887-0357

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18 of the United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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(See note
C above)

Inventor's Signature Kousuke Suzuki Date February 4, 1998

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Kawasaki-shi, Kanagawa, 211-8588 Japan

Full name of second inventor (given name, family name) Katsuyuki Karakawa

Inventor's Signature Katsuyuki Karakawa Date February 4, 1998

Residence Kasugai-shi, Aichi, Japan Citizenship Japan

Post Office Address c/o FUJITSU VLSI LIMITED, 1844-2, Kozoji-cho 2-chome, Kasugai-shi,
Aichi, 487-0013 Japan

Full name of third inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of fourth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of fifth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of sixth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of seventh inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

Full name of eighth inventor (given name, family name) _____

Inventor's Signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

FIG. 1A
PRIOR ART

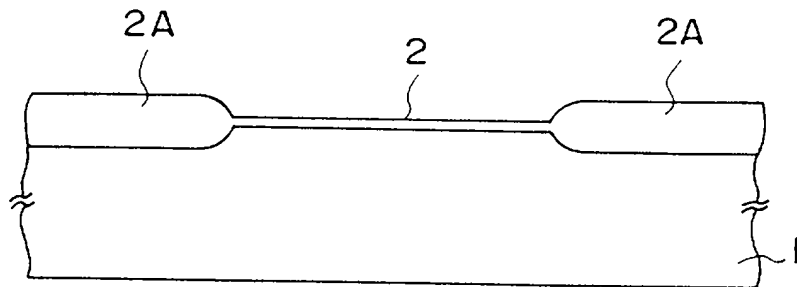


FIG. 1B
PRIOR ART

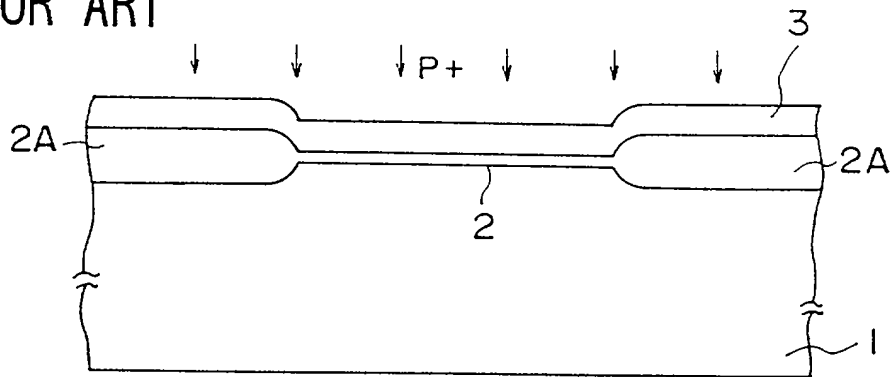


FIG. 1C
PRIOR ART

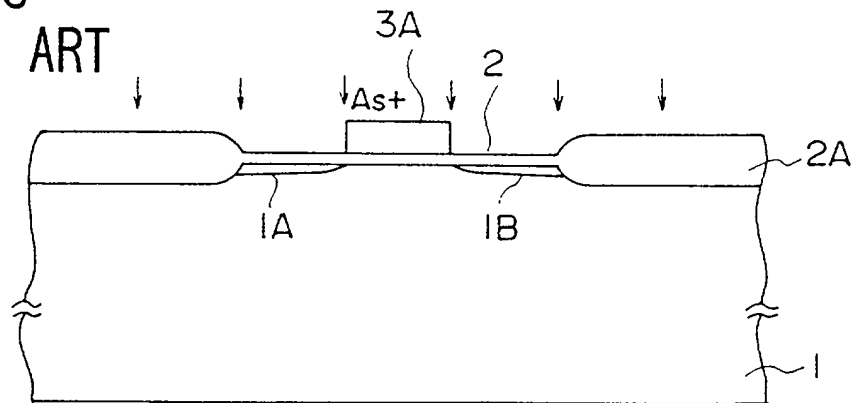


FIG. 1D
PRIOR ART

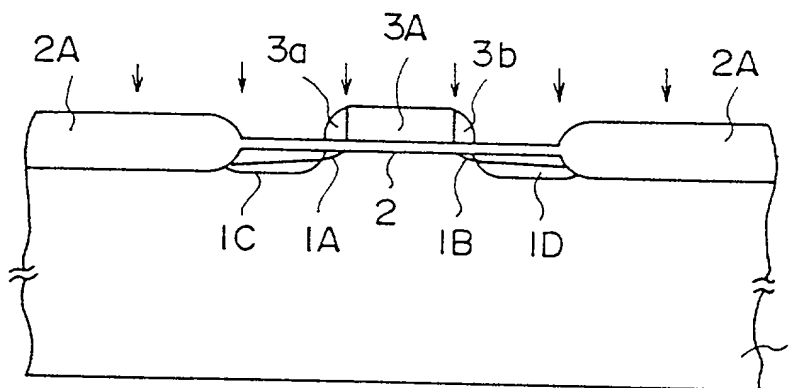


FIG. 1E
PRIOR ART

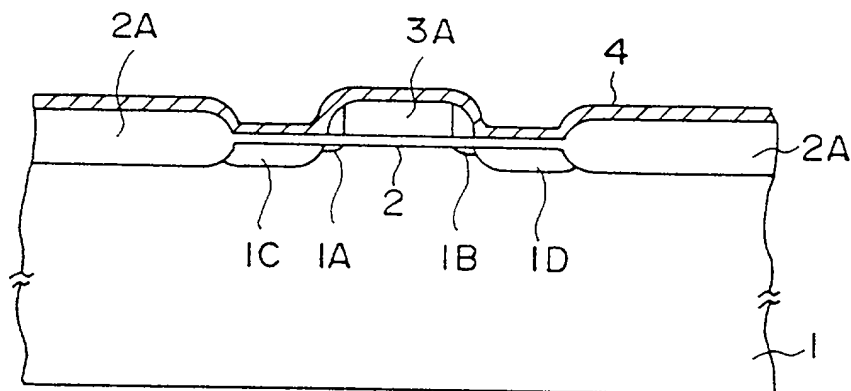


FIG. 1F
PRIOR ART

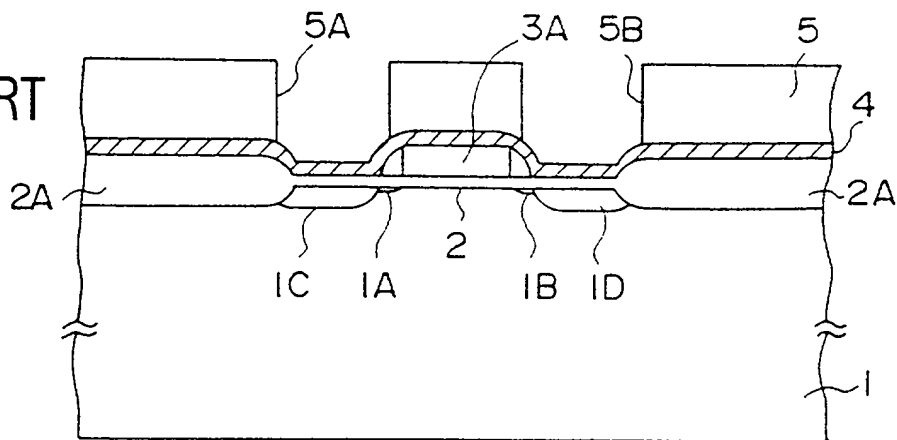


FIG. 1G
PRIOR ART

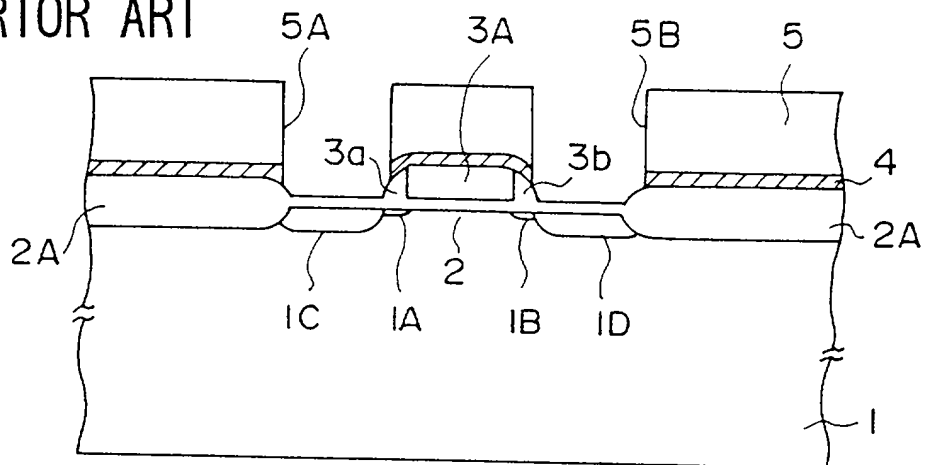


FIG. 1H
PRIOR ART

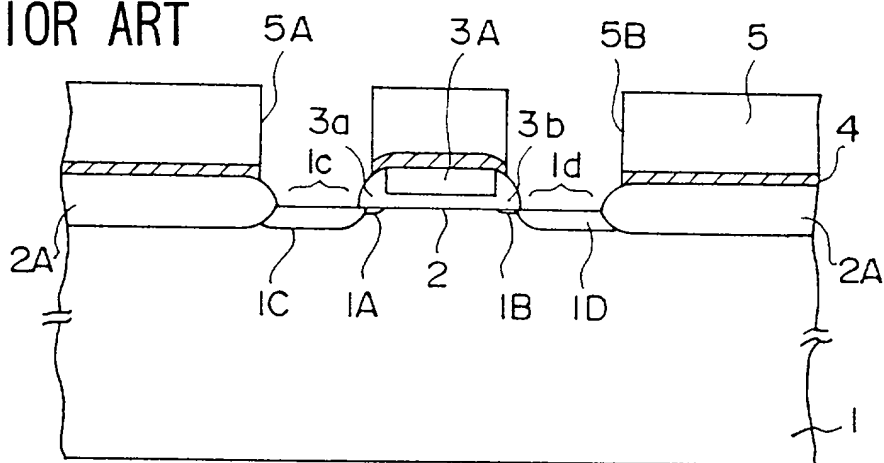


FIG. 2 PRIOR ART

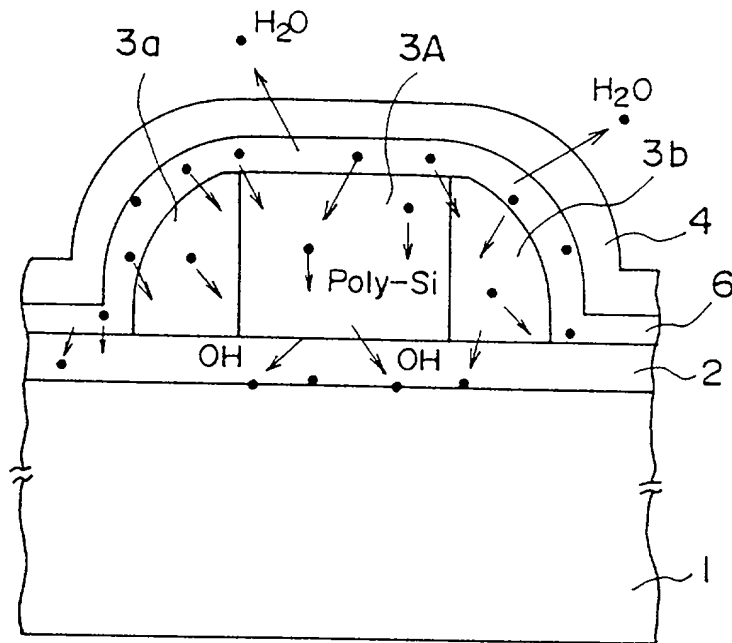


FIG. 3

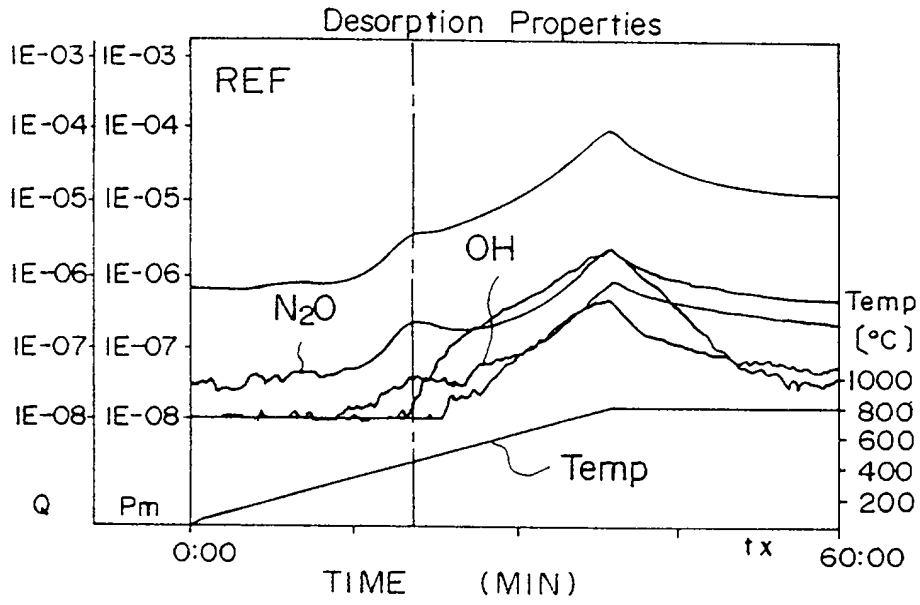


FIG. 4

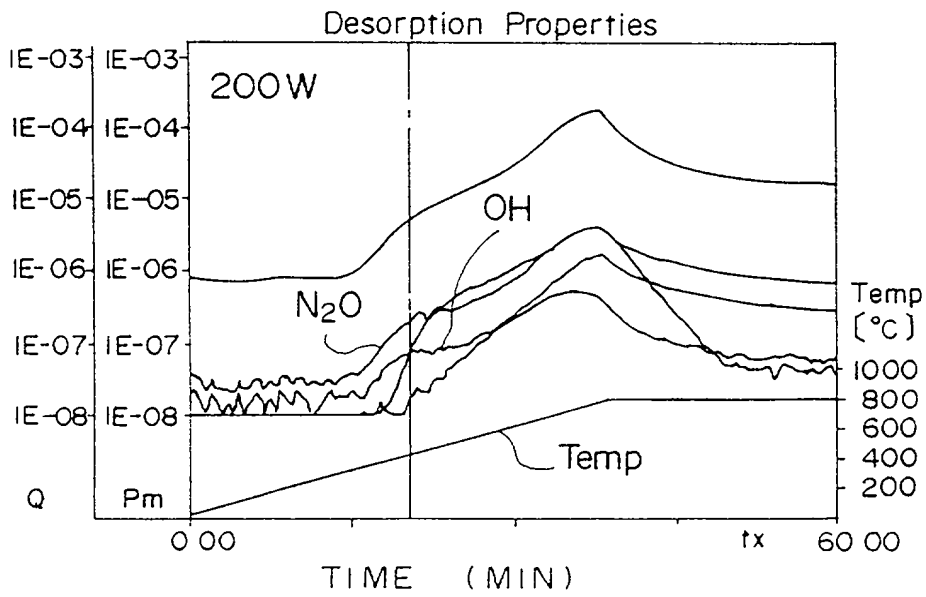


FIG. 5

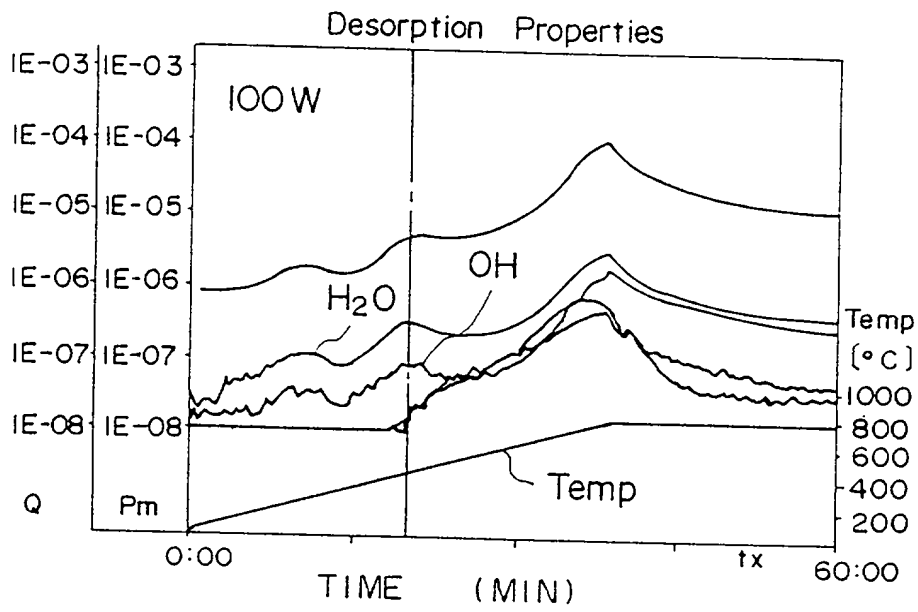


FIG. 6

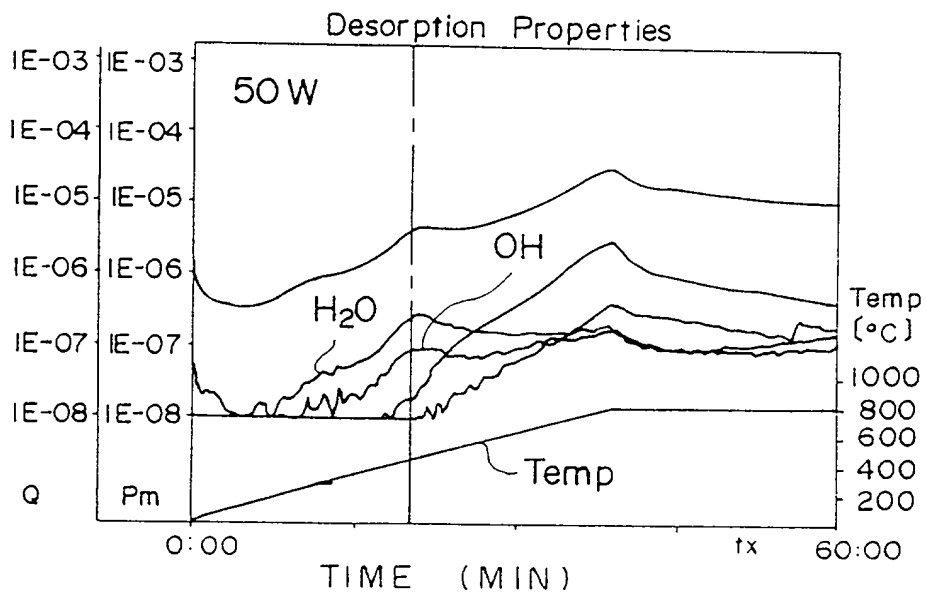


FIG. 7

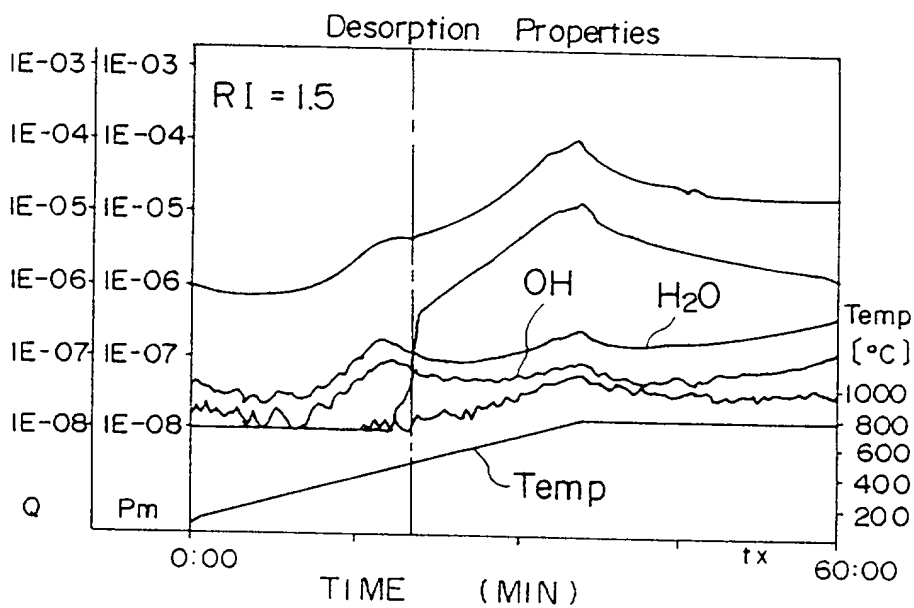


FIG. 8

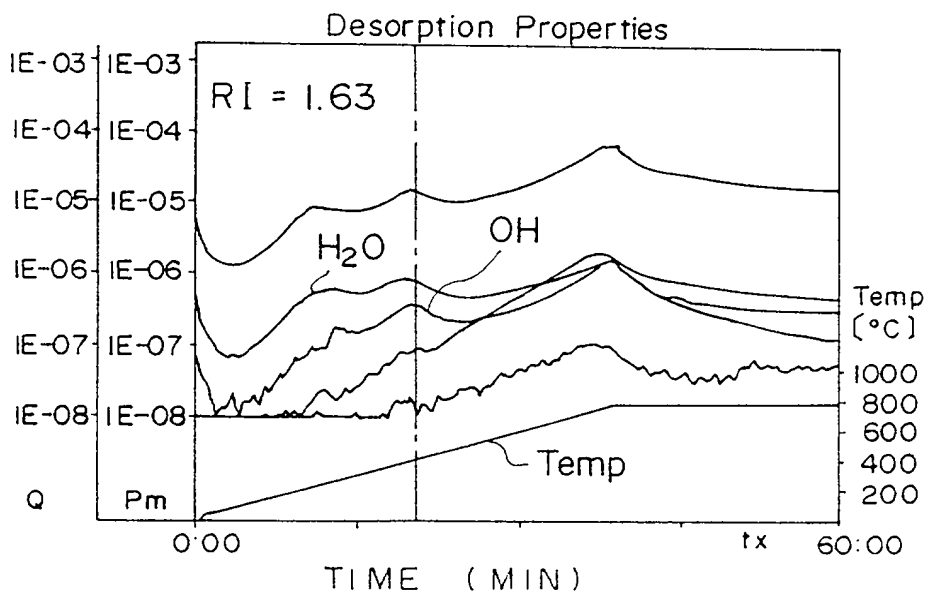


FIG. 9

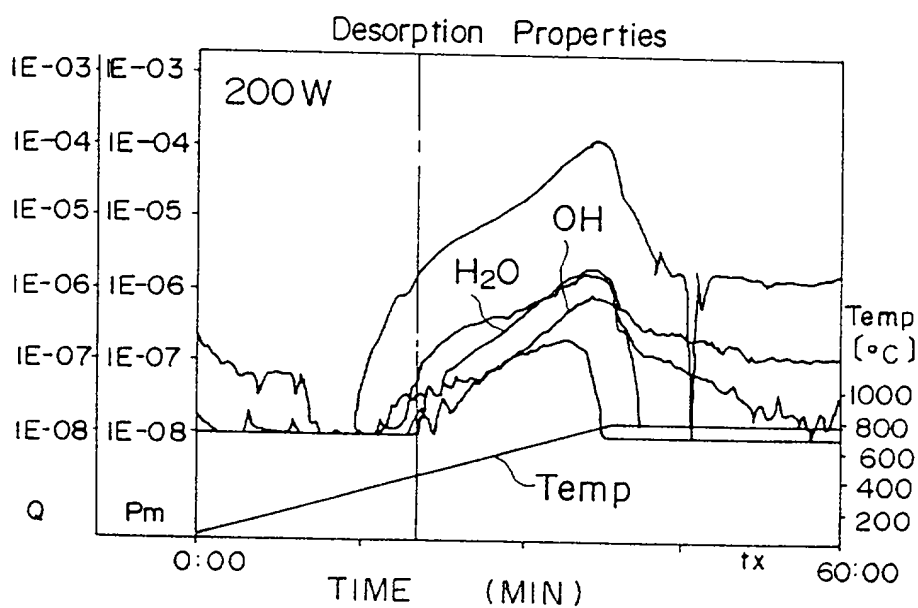


FIG. 10

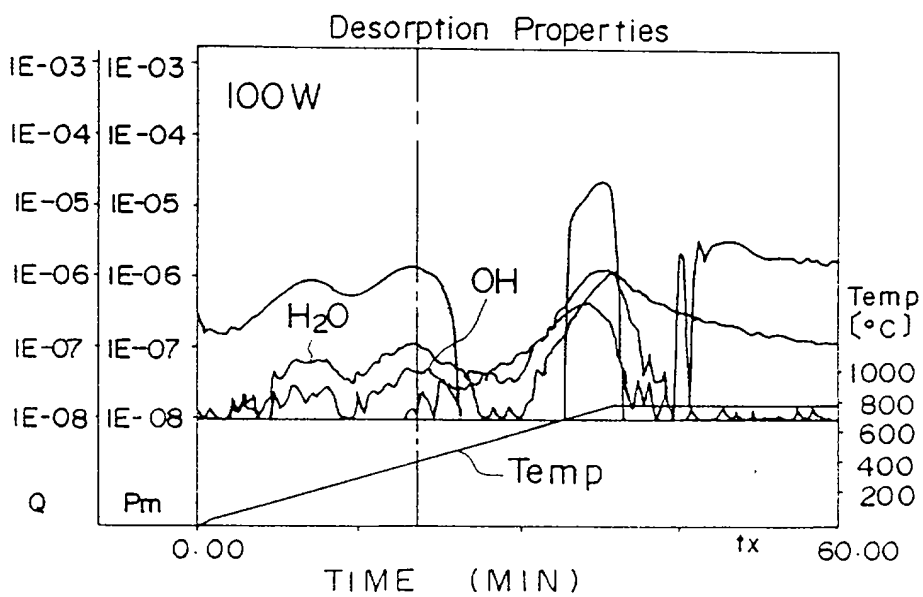


FIG. 11

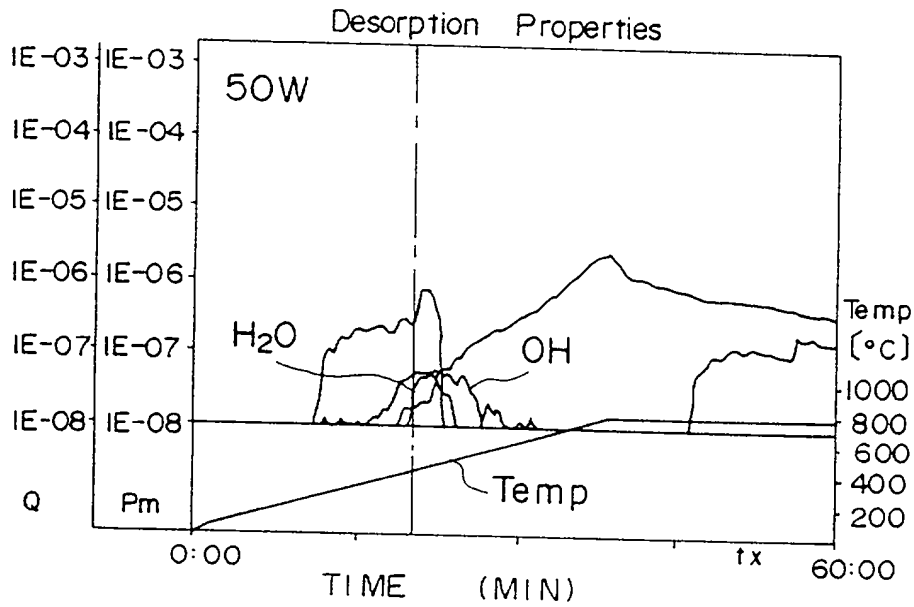
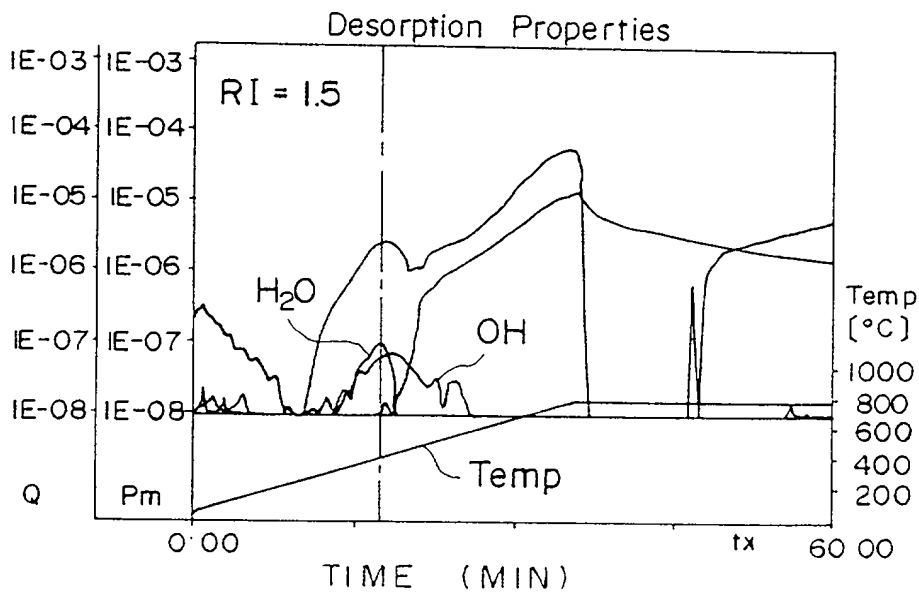


FIG. 12



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FIG. 13

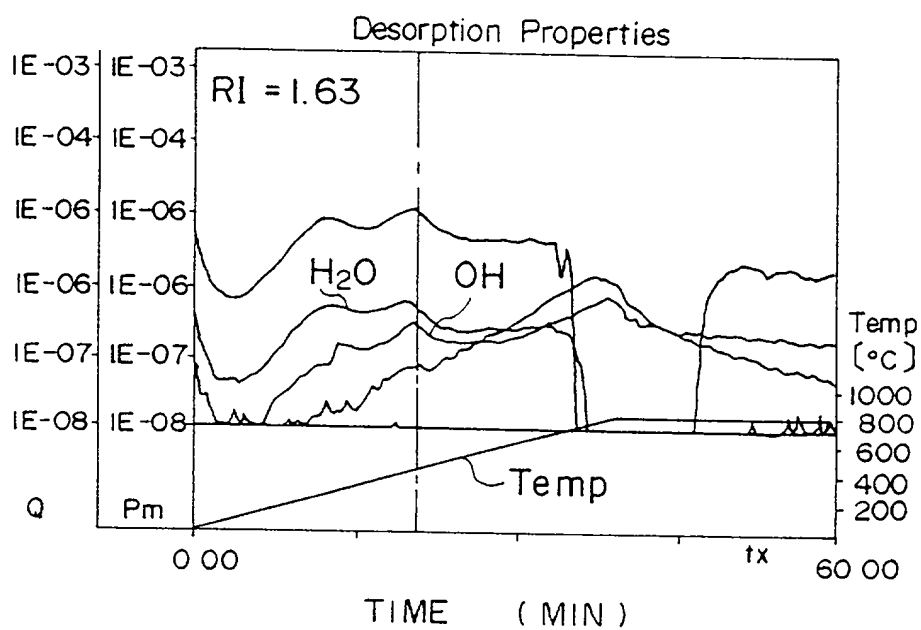


FIG. 14 PRIOR ART

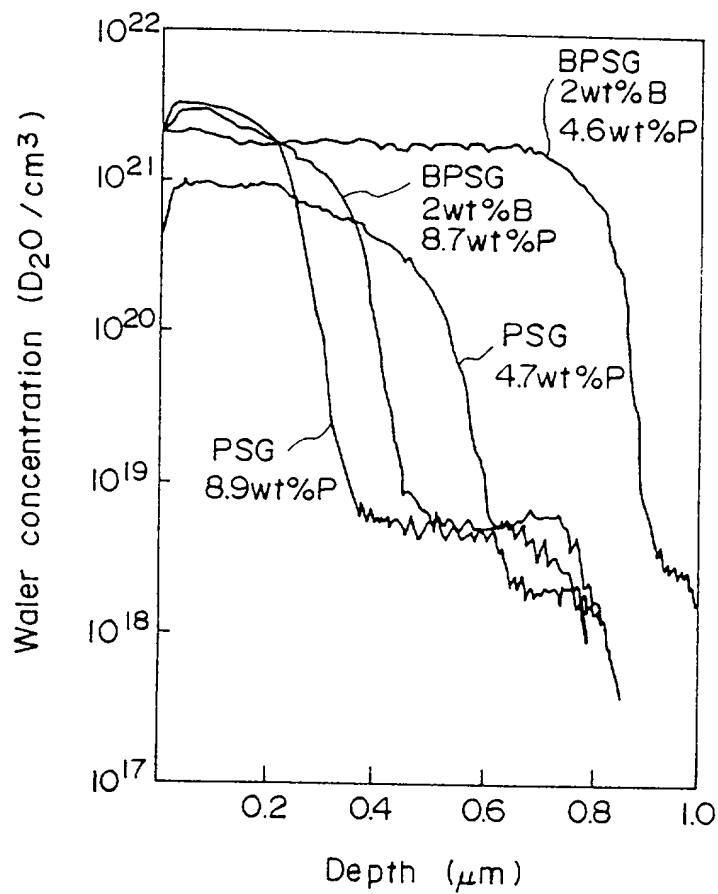


FIG. 15A

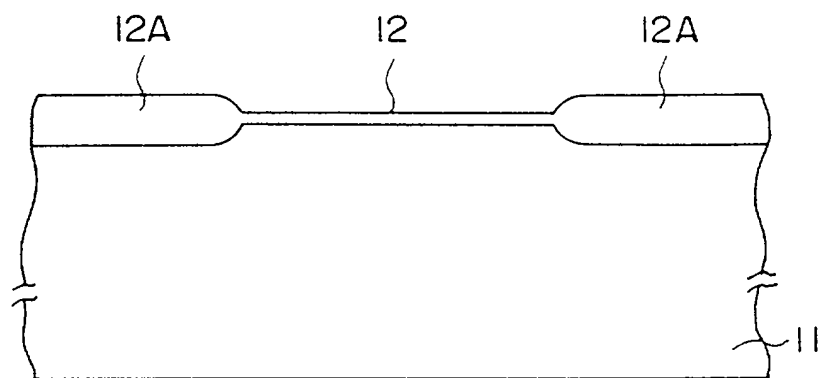


FIG. 15B

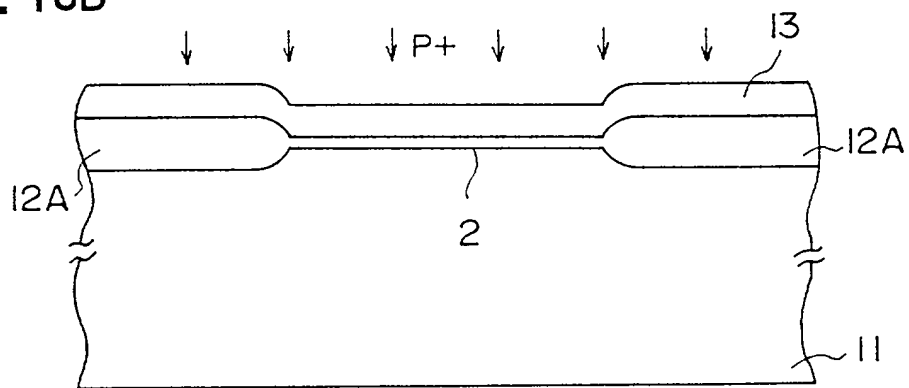


FIG. 15C

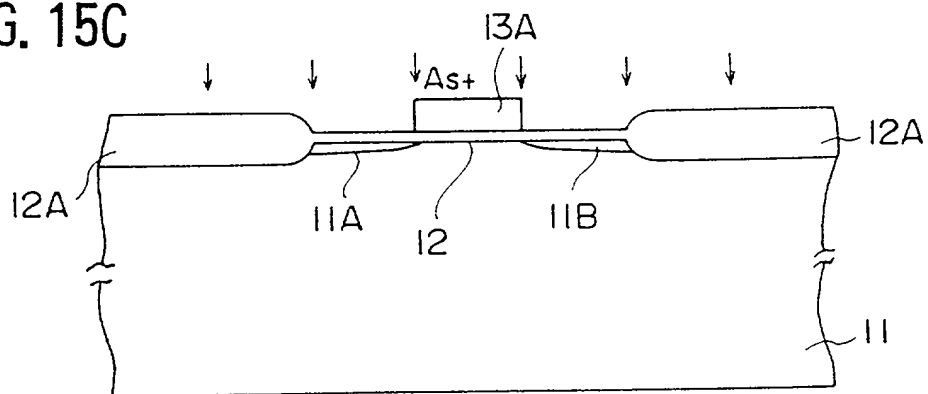


FIG. 15D

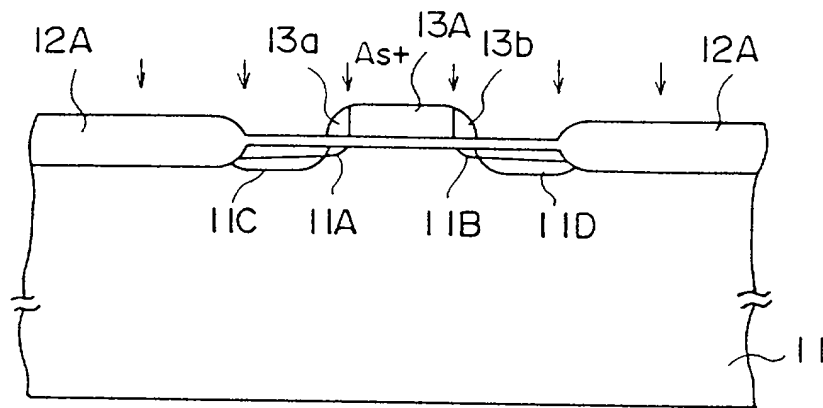


FIG. 15E

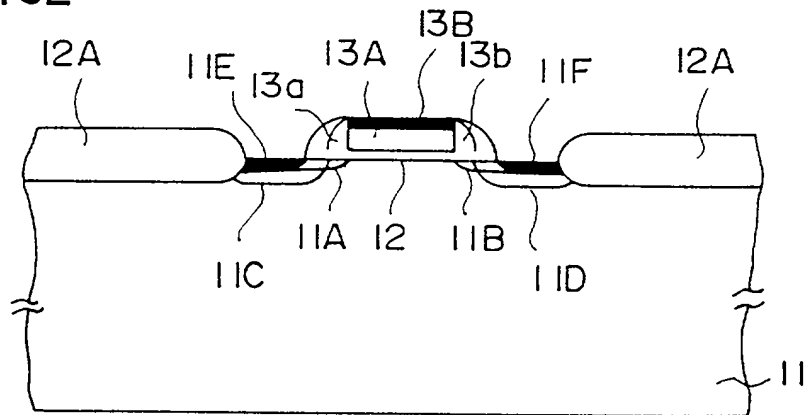


FIG. 15F

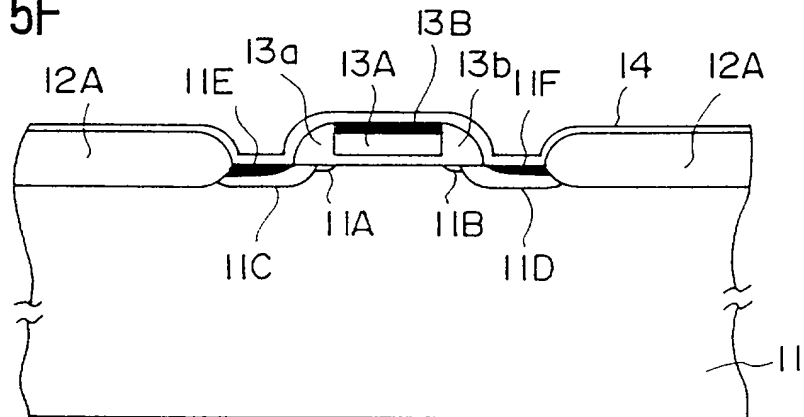


FIG. 15G

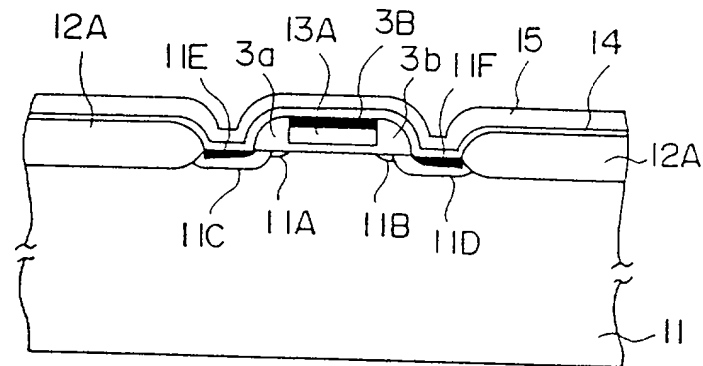


FIG. 15H

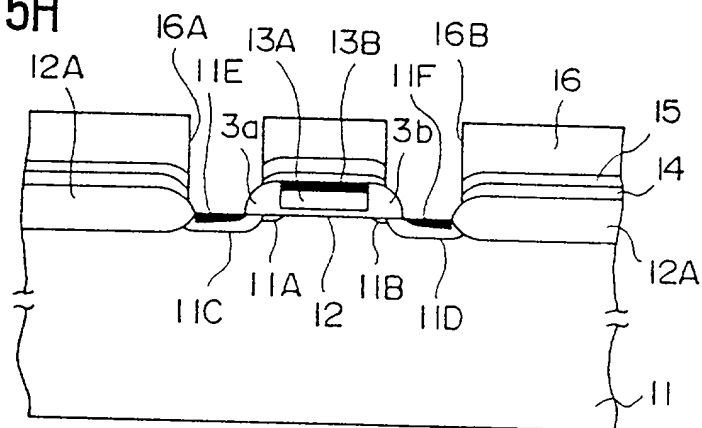


FIG. 15I

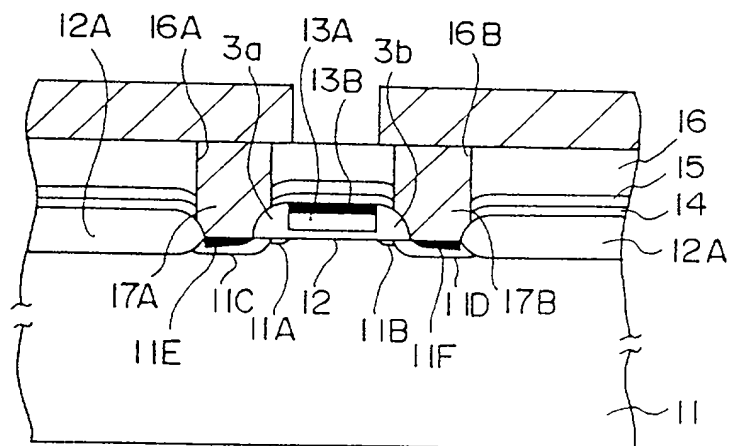


FIG. 16A

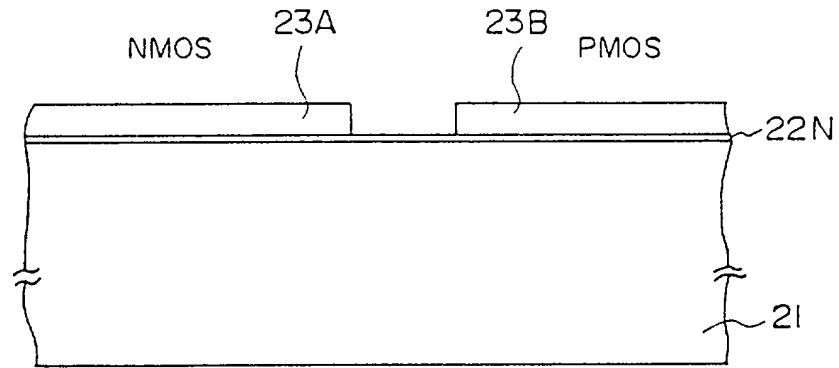


FIG. 16B

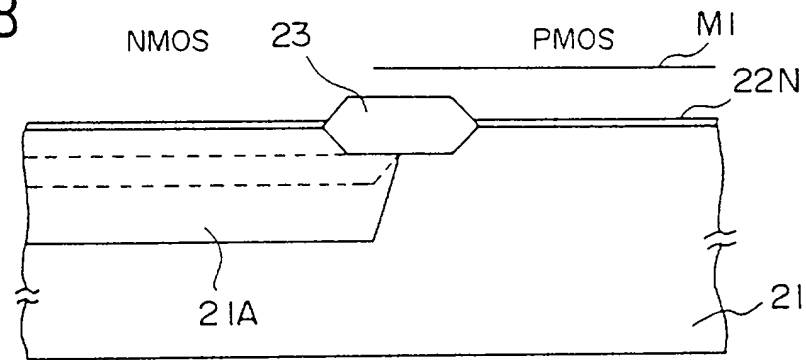


FIG. 16C

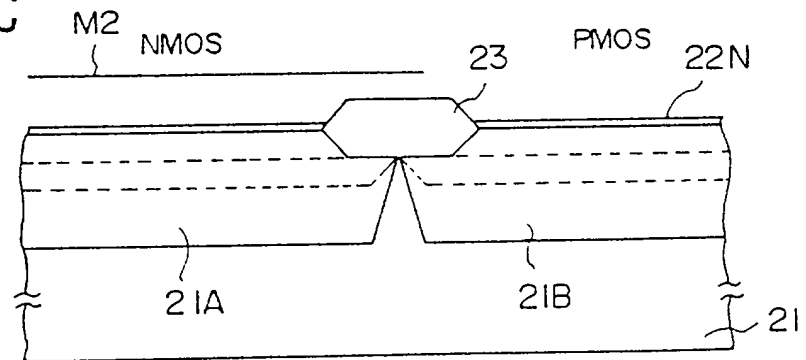


FIG. 16D

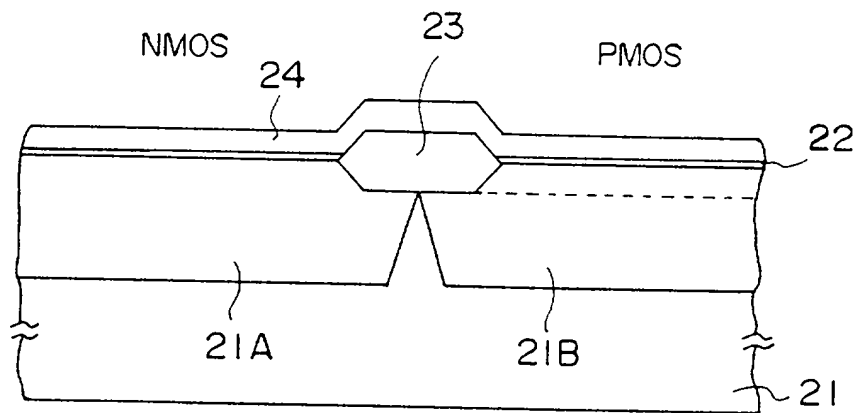


FIG. 16E

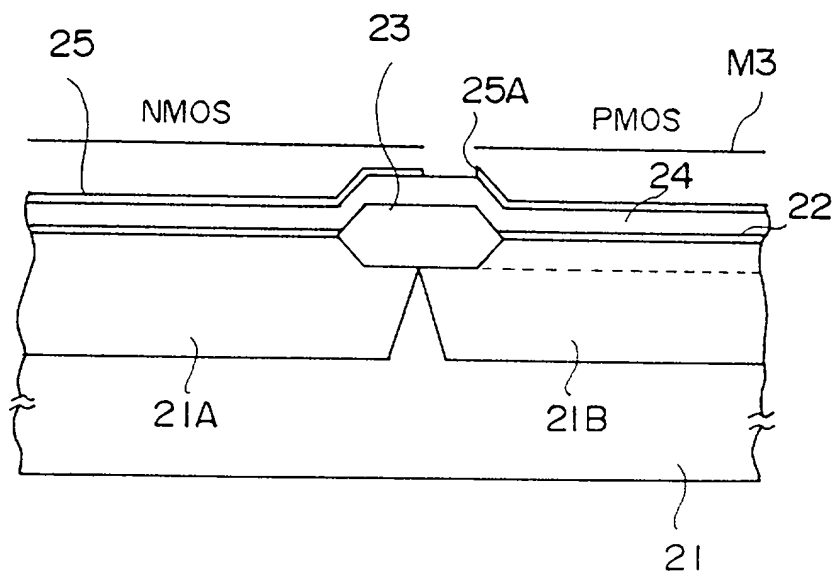


FIG. 16F

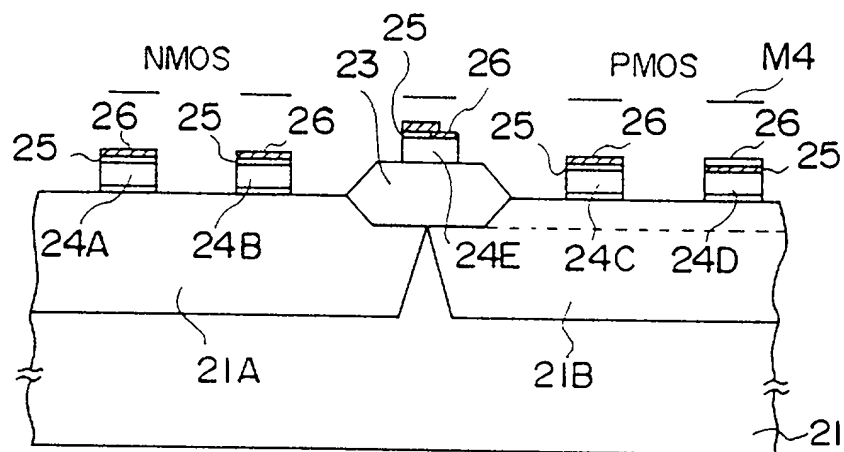


FIG. 16G

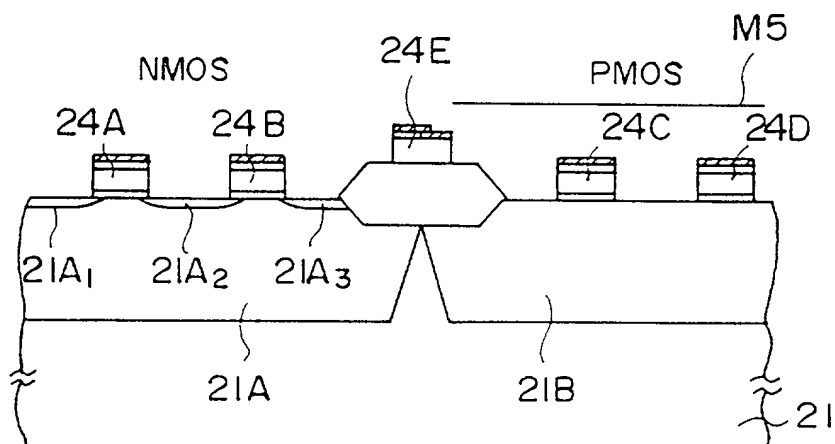


FIG. 16H

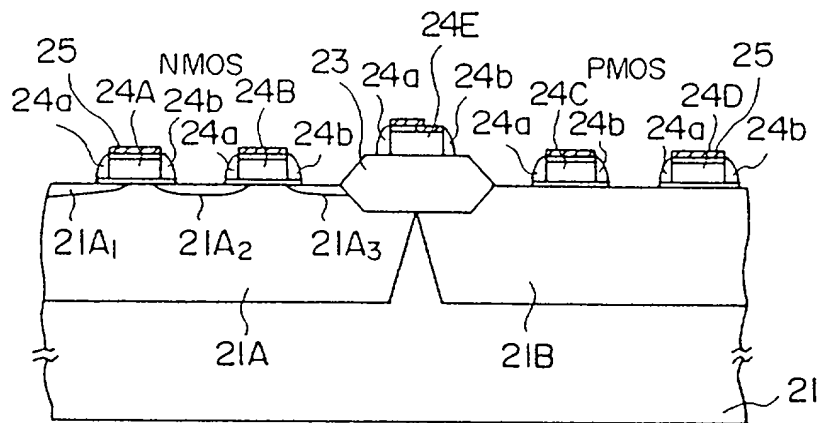


FIG. 16I

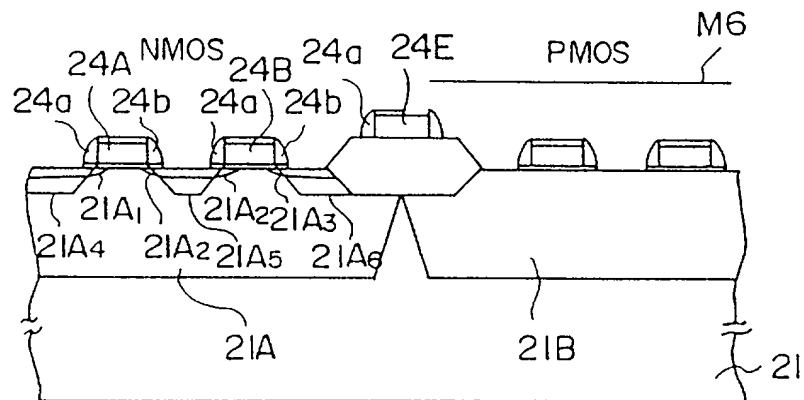


FIG. 16J

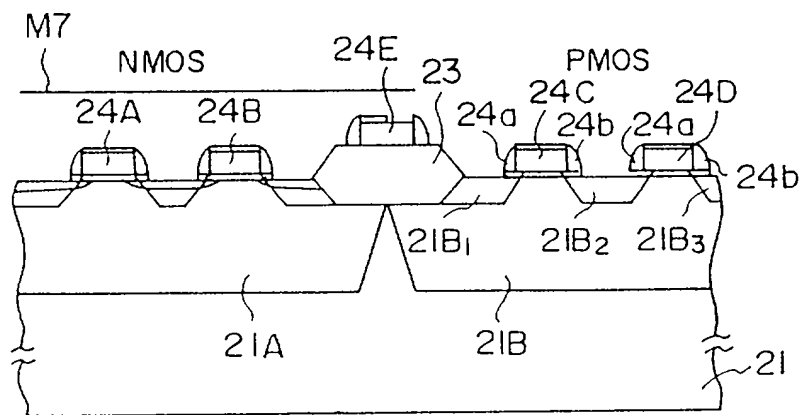


FIG. 16K

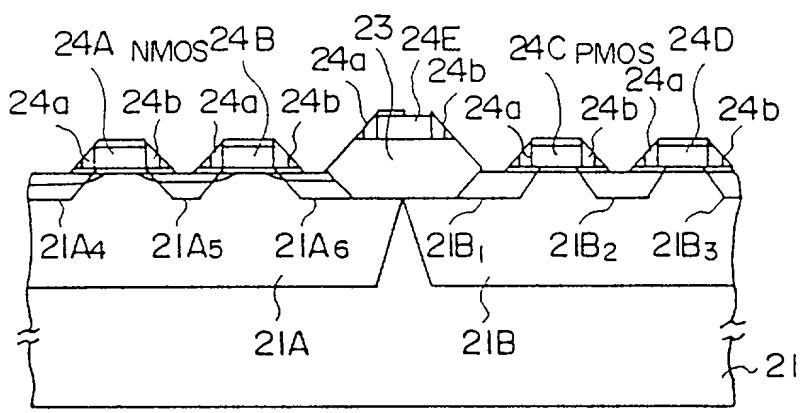


FIG. 16L

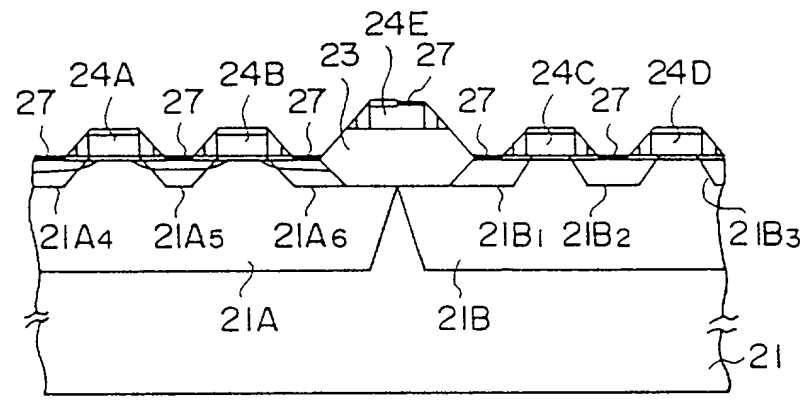
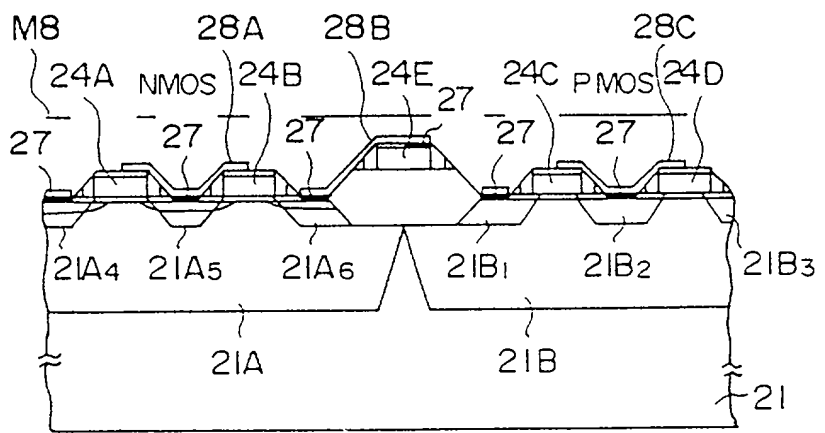


FIG. 16M



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FIG. 16N

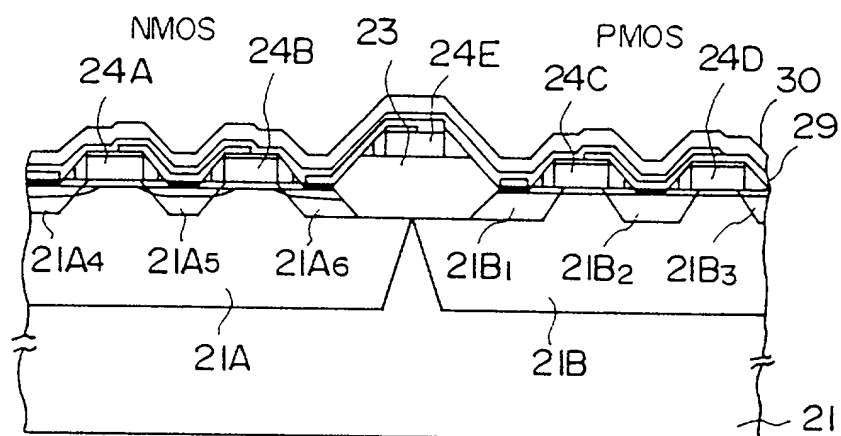


FIG. 16O

